ORDER NO.ISD0110009S0
G20

Service Manual

Front Counter Register

JS-170FR-**

Panasonic®

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⚠WARNING

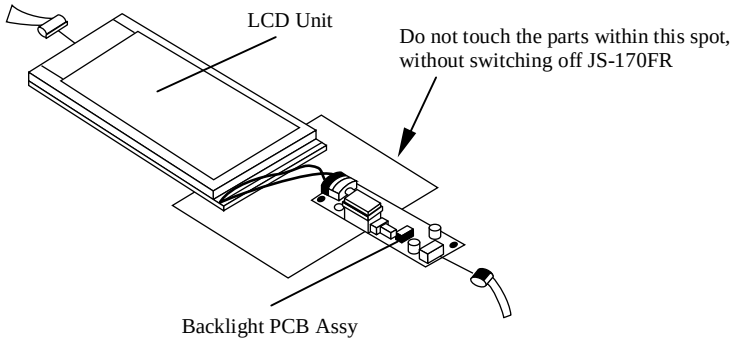
This service information is designed for experienced repair technicians only and is not designed for use by the general public. It does not contain warnings or cautions to advise non-technical should be potential dangers in attempting to service a product. Products powered by electricity should be serviced or repaired only by experienced professional technicians. Any attempt to service or repair the product or products dealt with in this service information by anyone could result in serious injury or death.

Design and specifications are subject to change without notice.

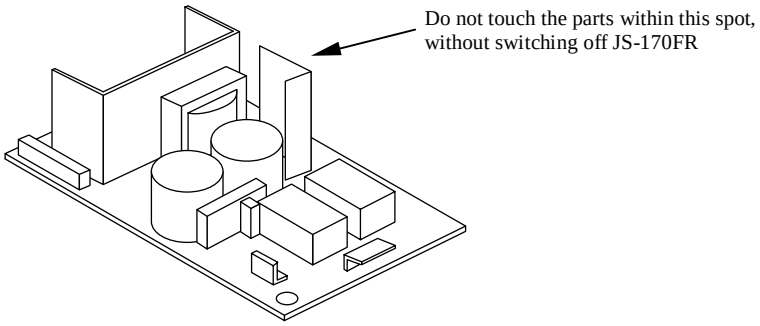
Caution

(1) High voltage is applied to inverter transformer, cable and capacitor on the backlight PCB and backlight connector shown in Fig. 1 below.
Do not touch those parts without switching off JS-170FR, expect for probes of oscilloscope or tester for testing or repairing purpose only.

Fig.1



(2) High voltage (230 V DC) is applied to heat sink (indicated by arrow) on Power Supply PCB Unit shown in the Figure below.
Do not touch this part without switching off JS-170FR



Power Supply PCB Unit

Design and specifications are subject to change without notice.

International Pentium POS Series Models are classified according to the systems shown below.

JS-170FR-X1, X2

- X2: Type of Specifications
- X1: Country Code

X1 Country Code

Code	Country or Area
E	England
G	Germany
F	European
A	Australia
W	Taiwan
U	U.S.A, Canda
S	Scandinavia
C	Canada

Type of JS-170FR Specifications

Model No.	Specification change timing	Country	Cap Color	RAM size (MB)	Battery	O/S	Dip SW (TP, MSR)	Customer Display	CPU	MSR	Other
JS-170FR-U20	From begin	USA	Yellow	64	O	N/A	Fujitsu, 1/2	O	266MHz	Not Standard	120V
↓	↓		↓	↓	↓	↓	↓	↓	↓	↓	
JS-170FR-U22	June,2001		Gray	64	O	N/A	Fujitsu, 1/2	O	266MHz	Not Standard	
↓	↓		↓	↓	↓	↓	↓	↓	↓	↓	
JS-170FR-U24	September,2001		Gray	64	O	N/A	Fujitsu, 1/2	O	333MHz	Not Standard	
JS-170FR-U21	From begin	USA	Yellow	64	O	N/A	Fujitsu, 1/2	×	266MHz	Not Standard	120V
↓	↓		↓	↓	↓	↓	↓	↓	↓	↓	
JS-170FR-U23	June,2001		Gray	64	O	N/A	Fujitsu, 1/2	×	266MHz	Not Standard	
↓	↓		↓	↓	↓	↓	↓	↓	↓	↓	
JS-170FR-U25	September,2001		Gray	64	O	N/A	Fujitsu, 1/2	×	333MHz	Not Standard	
JS-170FR-G20	From begin	Germany	Yellow	16	O	DOS 6.22	Gen, 2	O	266MHz	Not Standard	AC Cable Straight
↓	↓		↓	↓	↓	↓	↓	↓	↓	↓	↓
JS-170FR-G22	July,2001		Friendly Gray	64	O	DOS 6.22	Gen, 2	O	266MHz	Standard	AC Cable L type
↓	↓		↓	↓	↓	↓	↓	↓	↓	↓	
JS-170FR-G24	September,2001		Friendly Gray	64	O	DOS 6.22	Gen, 2	O	333MHz	Standard	
JS-170FR-G21	From begin	Germany	Yellow	16	O	DOS 6.22	Gen, 2	×	266MHz	Not Standard	AC Cable Straight
↓	↓		↓	↓	↓		↓	↓	↓	↓	↓
JS-170FR-G23	July,2001		Friendly Gray	64	O	DOS 6.22	Gen, 2	×	266MHz	Standard	AC Cable L type
↓	↓		↓	↓	↓		↓	↓	↓	↓	
JS-170FR-G25	September,2001		Friendly Gray	64	O	DOS 6.22	Gen, 2	×	333MHz	Standard	
JS-170FR-E20	From begin	UK	Yellow	64	O	N/A	Fujitsu, 1/2	O	266MHz	Not Standard	
↓	↓		↓	↓	↓	↓	↓	↓	↓	↓	
JS-170FR-E22	June,2001		Gray	64	O	N/A	Fujitsu, 1/2	O	266MHz	Not Standard	
↓	↓		↓	↓	↓	↓	↓	↓	↓	↓	
JS-170FR-E24	September,2001		Gray	64	O	N/A	Fujitsu, 1/2	O	333MHz	Standard	

Model No.	Specification change timing	Country	Cap Color	RAM size (MB)	Battery	O/S	Dip SW (TP, MSR)	Customer Display	CPU	MSR	Other
JS-170FR-E21	From begin	UK	Yellow	64	O	N/A	Fujitsu, 1/2	×	266MHz	Not Standard	
↓	↓		↓	↓	↓	↓	↓	↓	↓	↓	
JS-170FR-E23	June,2001		Gray	64	O	N/A	Fujitsu, 1/2	×	266MHz	Not Standard	
↓	↓		↓	↓	↓	↓	↓	↓	↓	↓	
JS-170FR-E25	September,2001		Gray	64	O	N/A	Fujitsu, 1/2	×	333MHz	Standard	
JS-170FR-S20	From begin	Scandinavia	Yellow	64	O	N/A	Fujitsu, 1/2	O	266MHz	Not Standard	
↓	↓		↓	↓	↓	↓	↓	↓	↓	↓	
Discontinue	June,2001		N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	
JS-170FR-F22	June,2001	European	Gray	64	O	N/A	Fujitsu, 1/2	O	266MHz	Not Standard	AC Cable L type
↓	↓		↓	↓	↓	↓	↓	↓	↓	↓	
JS-170FR-F24	September,2001		Gray	64	O	N/A	Fujitsu, 1/2	O	333MHz	Standard	
JS-170FR-F23	June,2001	European	Gray	64	O	N/A	Fujitsu, 1/2	×	266MHz	Not Standard	AC Cable L type
↓	↓		↓	↓	↓	↓	↓	↓	↓	↓	
JS-170FR-F25	September,2001		Gray	64	O	N/A	Fujitsu, 1/2	×	333MHz	Standard	
JS-170FR-A20	From begin	Australia	Yellow	16	O	DOS 6.22	Gen, 2	O	266MHz	Not Standard	
↓	↓		↓	↓	↓	↓	↓	↓	↓	↓	
JS-170FR-A22	June,2001		Gray	64	O	N/A	Fujitsu, 1/2	O	266MHz	Not Standard	
↓	↓		↓	↓	↓	↓	↓	↓	↓	↓	
JS-170FR-A24	September,2001		Gray	64	O	N/A	Fujitsu, 1/2	O	333MHz	Standard	
JS-170FR-A23	June,2001	Australia	Gray	64	O	N/A	Fujitsu, 1/2	×	266MHz	Not Standard	
↓	↓		↓	↓	↓	↓	↓	↓	↓	↓	
JS-170FR-A25	September,2001		Gray	64	O	N/A	Fujitsu, 1/2	×	333MHz	Standard	
JS-170FR-W20	From begin	Taiwan	Yellow	16	O	DOS 6.22	Gen, 2	O	266MHz	Not Standard	120V
↓	↓		↓	↓	↓	↓	↓	↓	↓	↓	
JS-170FR-W22	June,2001		Gray	64	O	N/A	Fujitsu, 1/2	O	266MHz	Not Standard	
↓	↓		↓	↓	↓	↓	↓	↓	↓	↓	
JS-170FR-W24	September,2001		Gray	64	O	N/A	Fujitsu, 1/2	O	333MHz	Standard	
JS-170FR-W23	June,2001	Taiwan	Gray	64	O	N/A	Fujitsu, 1/2	×	266MHz	Not Standard	120V
↓	↓		↓	↓	↓	↓	↓	↓	↓	↓	
JS-170FR-W25	September,2001		Gray	64	O	N/A	Fujitsu, 1/2	×	333MHz	Standard	
JS-170FR-C24	April,2002	Canada	Gray	64	O	N/A	Fujitsu, 1/2	O	333MHz	Standard	120V
JS-170FR-C25	April,2002	Canada	Gray	64	O	N/A	Fujitsu, 1/2	×	333MHz	Standard	120V

Serial Number Control Table for Classified Modifications in the JR-170FR Models

			Model Number									
#	Modification	Description	U20,U21	U22,U23	U24,U25	G20,G21	G22,G23	G24,G25	E20,E21	E22,E23	E24,E25	S20,21
1	Main board modified	R430 jumper wire imbedded	01D*****	--------	--------	01D*****	--------	--------	01D*****	--------	--------	01D*****
2	Resistor R430 added	10 kilo-ohms added	01A*****	--------	--------	01A*****	--------	--------	01A*****	--------	--------	01A*****
3	Constant of resistor R181 modified	From 1.2 kilo-ohms to 750 ohms	01A*****	--------	--------	01A*****	--------	--------	01A*****	--------	--------	01A*****
4	DIMM enhanced	From 16 MB to 64 MB	01B*****	--------	--------	01B*****	--------	--------	01B*****	--------	--------	01B*****
5	Baud rate of customer display enhanced	From 2400 bps to 9600 bps (except G version)	01B*****	--------	--------	01B*****	--------	--------	01B*****	--------	--------	01B*****
6	Operating System	Not pre-installed (except G version)	01B*****	--------	--------	01B*****	--------	--------	01B*****	--------	--------	01B*****
7	Power supply modified	Manufacturer changed	01D*****	--------	--------	01D*****	--------	--------	01D*****	--------	--------	01D*****
8	Power supply modified	Diffuser panel added	--------	--------	02A*****	--------	--------	02A*****	--------	--------	02A*****	--------
9	CN1	Not implemented	01D*****	--------	--------	01D*****	--------	--------	01D*****	--------	--------	01D*****
10	IDE interface buffer	IC18-23 not implemented	01D*****	--------	--------	01D*****	--------	--------	01D*****	--------	--------	01D*****
11	LAN LSI driver software version-up	LSI manufacturer demand	--------	01J*****	--------	--------	01J*****	--------	--------	01J*****	--------	--------
12	Hard disk enhanced	From 3.25 GB to 5 GB	--------	01F*****	--------	--------	01F*****	--------	--------	01F*****	--------	--------
13	LAN driver software	Software modified	--------	01J*****	--------	--------	01J*****	--------	--------	01J*****	--------	--------
14	Lower case modified (1)	Battery replacement simplified	00N*****	--------	--------	00H*****	--------	--------	00F*****	--------	--------	00N*****
15	Lower case modified (2)	Rubber foot frame reinforced	--------	--------	02B*****	--------	--------	02B*****	--------	--------	02B*****	--------

			Model Number									
#	Modification	Description	F22,F23	F24,F25	A20,A21	A22,A23	A24,A25	W20,W21	W22,W23	W24,W25	C24,C25	
1	Main board modified	R430 jumper wire imbedded	--------	--------	01D*****	--------	--------	01D*****	--------	--------	--------	
2	Resistor R430 added	10 kilo-ohms added	--------	--------	01A*****	--------	--------	01A*****	--------	--------	--------	
3	Constant of resistor R181 modified	From 1.2 kilo-ohms to 750 ohms	--------	--------	01A*****	--------	--------	01A*****	--------	--------	--------	
4	DIMM enhanced	From 16 MB to 64 MB	--------	--------	01B*****	--------	--------	01B*****	--------	--------	--------	
5	Baud rate of customer display enhanced	From 2400 bps to 9600 bps (except G version)	--------	--------	01B*****	--------	--------	01B*****	--------	--------	--------	
6	Operating System	Not pre-installed (except G version)	--------	--------	01B*****	--------	--------	01B*****	--------	--------	--------	
7	Power supply modified	Manufacturer changed	--------	--------	01D*****	--------	--------	01D*****	--------	--------	--------	
8	Power supply modified	Diffuser panel added	--------	02A*****	--------	--------	02A*****	--------	--------	02A*****	02A*****	
9	CN1	Not implemented	--------	--------	01D*****	--------	--------	01D*****	--------	--------	--------	
10	IDE interface buffer	IC18-23 not implemented	--------	--------	01D*****	--------	--------	01D*****	--------	--------	--------	
11	LAN LSI driver software version-up	LSI manufacturer demand	01J*****	--------	--------	01J*****	--------	--------	01J*****	--------	--------	
12	Hard disk enhanced	From 3.25 GB to 5 GB	01F*****	--------	--------	01F*****	--------	--------	01F*****	--------	--------	
13	LAN driver software	Software modified	01J*****	--------	--------	01J*****	--------	--------	01J*****	--------	--------	
14	Lower case modified (1)	Battery replacement simplified	--------	--------	00F*****	--------	--------	00A*****	--------	--------	--------	
15	Lower case modified (2)	Rubber foot frame reinforced	--------	02B*****	--------	--------	02B*****	--------	--------	02B*****	02B*****	

Modification No.	Reason for modification
1	R430 jumper wire imbedded
2	Measures against locking up during LAN communication
3	Brightened CRT connected to VGA output
4	User demand
5	User demand
6	User demand
7	Attainment of stable parts supplier
8	Holding down temperature rise of stainless case
9	Elimination of connector for debugging
10	Elimination of Ultra DMA trouble
11	Ceased production of the part
12	Better marketability
13	TP slowdown
14	User demand
15	Prevention of rubber foot frame from being broken

• How to read serial numbers (starting month of modifying the specifications)

Ex.)

Example) 02 A *****

- ***** → Production number
- A → Production month (A = January)
- 02 → Production year (2002)

A = January
B = February
C = March
D = April
E = May
F = June
H = July
J = August
K = September
L = October
M = November
N = December

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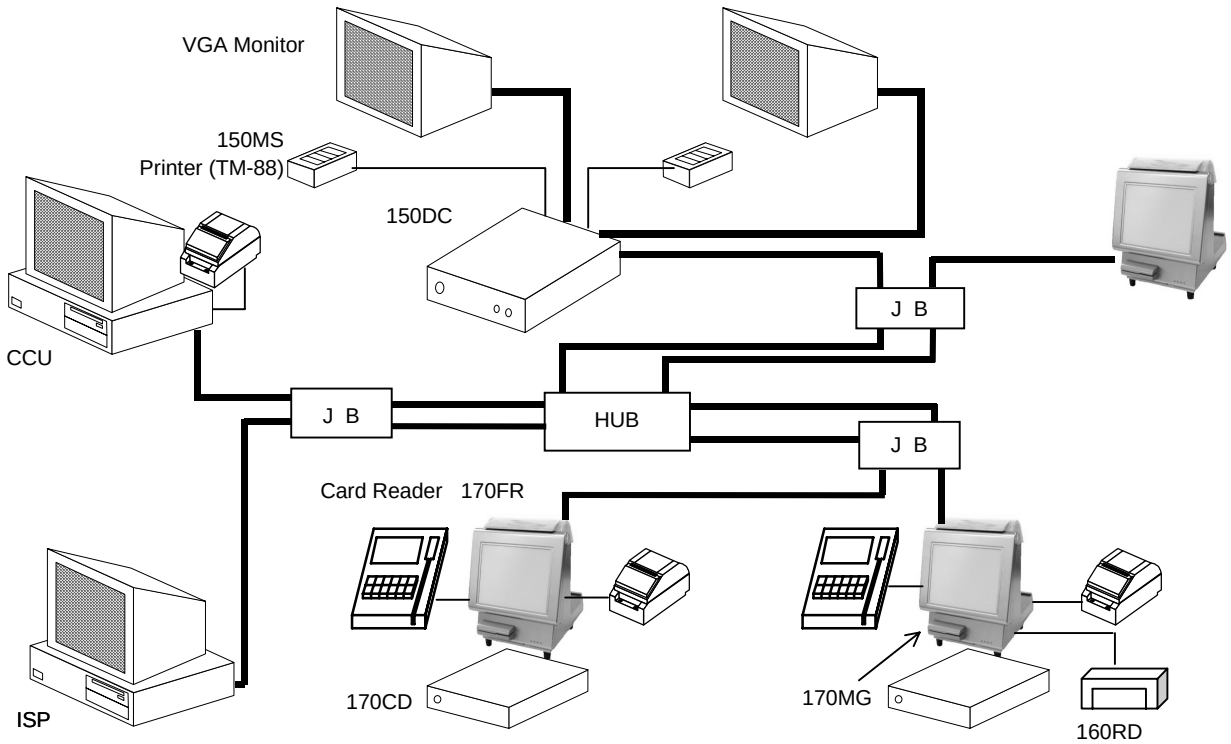
6.1 Packing 6-1

1 OVERVIEW

General

This model has the performance equivalent to an IBM-AT machine which uses the Pentium •as a CPU.
This model has its unique functions added to it and is provided with an ETHERNET circuit and touch panel as standard. The desired system can be built by adding various optional functions. Its display is of 800 x 600 SVGA specifications (standard), using a color LCD. It is provided with a 20-digit x 1-line or 2-line fluorescent display tube for customer display. In addition, it has an interface of up to 2 channels for a Cash Drawer.

System Configurations (Example)



CCU: Communication Control Unit
ISP: In-Store Processor
170FR: Front counter Register
150DC: Drive Through Controller
170CD: Cash Drawer
150MS: Bump Bar
160RD: Remote Display
170MG: Card Reader

Specifications

♦ Processor, Chipset and BIOS

CPU	Intel Mobile Pentium II 266MHz or 333 MHz (BGA1) CORE + 1.6V
Chipset	Intel 440BX/PIIX4E
BIOS	Phoenix BIOS

♦ Memory

- Main memory

Capacity	64MB Standard 256MB Maximum
Slot	168pin DIMM Slot x 2 One slot occupied by standard memory
Type	3.3V SDRAM supported

Note

- One 64MB SDRAM is mounted on socket-1 as factory standard.
- Each slot can have 16 MB (minimum) to 128 MB (maximum) memory module.
- Maximum height of DIMM is 35.65mm.
- EDO isn't being supported.

- L2 Cache (Secondary Cache)

  256KB on CPU die

- Video memory

  4MB in VGA Controller (Not expandable)

- BIOS ROM

Capacity	512KB
Type	Flash memory (Fujitsu MBM29F040 or compatible)

♦ Drives

Floppy disk drive	Option, external	One 3.5 type drive unit (1.44MB/720KB)
Hard disk drive	Standard, internal	One 2.5 type EIDE drive unit (4.0GB or more)
	Option, internal	One 2.5 type EIDE drive unit

♦ Clock

Tolerance	Monthly ± 3 minutes (Temperature 25°C)

♦ Back-up Method

- Real Time Clock (RTC)

Battery	Lithium battery, 560mAh
Battery life	8 years (need to be changed every 8 years)
Retention time	8 years (On condition that unit is turned on for 12 hours per a day)

- Power supply

Battery	Ni-Cd battery, 1200mAh
Battery life	2 years(need to be changed every 2 years)
Retention time	2 minutes - On condition that the battery is fully charged at installation (Registers must be powered on for more than 72 hours for full battery charge) - No display on the LCD during AC off

♦ Display

- Crew display

Display unit	TFT type LCD with Dual Back Light
Resolution	800 x 600 (SVGA)
Dot pitch	0.3 mm
Display size	12.1 type
Contrast adjust	Not needed

- Customer display

Display unit	Fluorescent display tube
Color	Green
Number of digits	20 characters (5 x 7dots, 9 x 6 mm) x 2 lines
Interface	Serial shared with COM3 (TTL level) (It is possible to switch between Customer Display and External COM3 port by software)

♦ Touch Panel

Type	Resistive
Life	Resistive over 10 million times by finger touch (Simulates human finger, Shape of rubber end:R8, Hardness:60°, Load:200g, Frequency:5 Hz)
Interface	Serial interface (using internal COM4, TTL level)
Size	12.1 type

♦ Local Area Network

Interface	Ethernet (10BASE-T/100BASE-TX)
Speed	10M /100Mbps
Connector	8-pin Modular Jack (RJ-45)
Wake on LAN	Supported

♦ Magnetic Card Reader (Option:U24/U25 type)

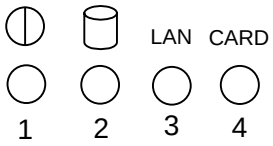
Track	ISO1/ISO2
Swipe speed	10 - 120 (maximum) cm/s Maximum swipe speed will be reduced when dual track reader is used.
Interface	Data is received as keyboard data
Limitation	On MS-DOS, magnetic card reader doesn't work with USB keyboard.
Life	Over 1 million swipe

♦ Buzzer

Buzzer volume is fixed.

♦ LED

Four status indicators on front panel.



1	Power (Green : Running, Red : Stand-by)
2	Hard disk (Light on access)
3	LAN (Light on LAN activity)
4	Card Reader (Green : Good, Red : Error)

♦ Expansion Slot (Option)

Either one of the below can be added on main board as an expansion slot.

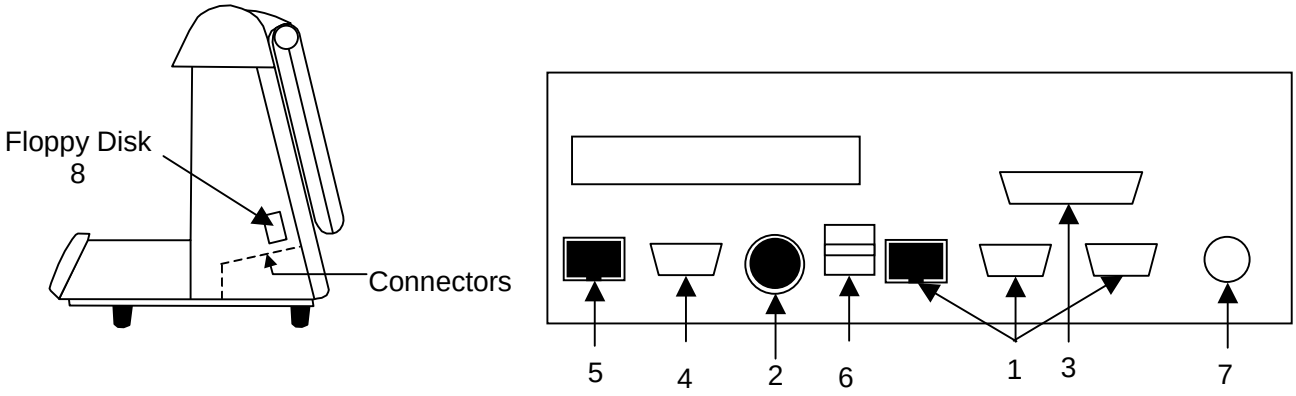
PCMCIA Slot	1 Type III or 2 Type II (Support PCMCIA/CardBus)
PCI Slot	1 PCI Bus Slot Maximum PCI card size (mm) : 174.63×106.68×(component side 14.48 + rear side 2.67)

♦ Supply Voltage

Voltage	100V system : AC 90V~132V 200V system : AC 198V~264V Depending on destination, Factory setting, Not changeable
Power consumption	Approx. 60W
Frequency	50/60 Hz

♦ Connectors

No	Interface	Number	Connector type
1	Serial	3	COM1/2 : 9pin D-sub connector, male COM3 : 8pin modular connector NOTE : COM3 is shared with Customer Display interface. (It is possible to switch between Customer Display and External COM3 port by software)
2	Cash Drawer	1	6pin DIN connector, female
3	Parallel	1	25pin D-SUB connector, female
4	Video	1	15pin D-SUB connector, female (VGA)
5	LAN	1	8-pin Modular Jack (RJ-45)
6	USB	2	USB Connector
7	Keyboard	1	6pin mini DIN connector
8	Floppy Disk	1	26pin mini I/O connector



See Appendix for pin assignments of each connector.

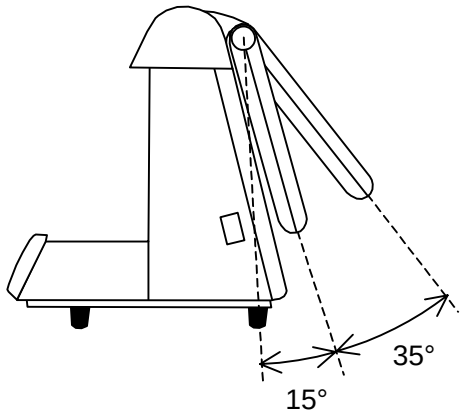
♦ Operation Condition

Temperature	5°C - 40°C (41°F - 104°F)
Humidity	20% RH - 85% RH (no dew)

♦ Dimension and Weight

Width	250 mm (9.8 inches) (Crew display : 312mm)
Depth	320 mm (12.6 inches)
Height	365 mm (14.4 inches) with rubber foot
Weight	Approx. 10 kg

Tilt angle



♦ Material

Case body	Stainless steel sheet
Top cover	ABS

♦ Supported OS

Microsoft MS-DOS, Windows 95, Windows NT Workstation 4.0

♦ Accessory

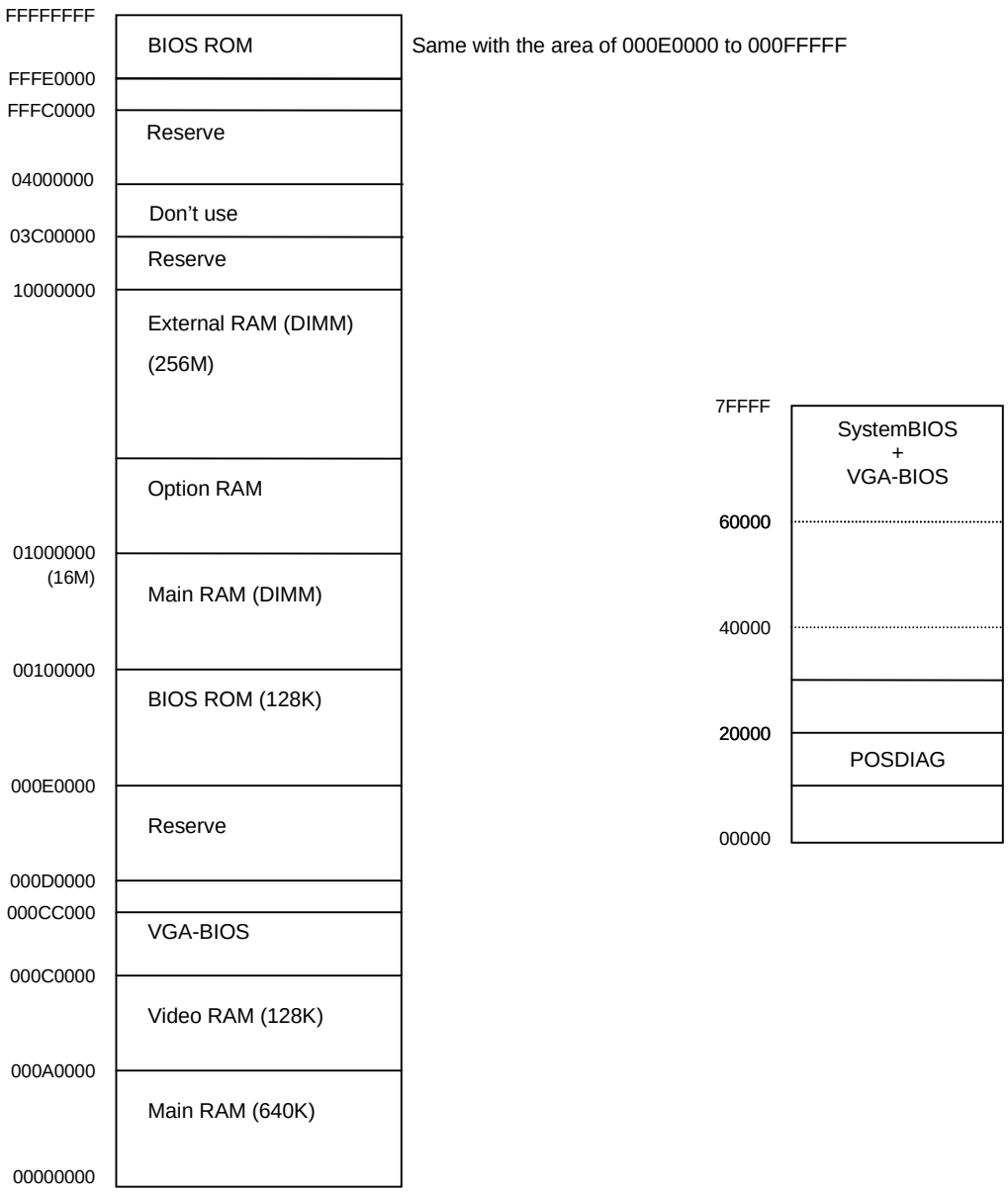
AC cable	1pc (2.5m)

♦ Safety Standard

Safety Standard.....TÜV
UL

EMI.....FCC Part15 Class A
CISPR Class B
CE
C-tick

Memory Map



Note: BIOS ROM always selects Bank0 after resetting the hardware.

I/O Port Map

Address (HEX)	Devices used for JS-170FR	
0000 - 001F	DMA Controller (1)	(82371EB)
0020 - 0021	Interrupt Controller (Master)	(82371EB)
0022 - 0023	443BX Chip Set	(82443BX)
0024 - 0027	Reserve	
0040 - 005F	Timer Controller	(82371EB)
0060 - 006F	Keyboard Controller	(IT8763F)
0070 - 007F	RTC, NMI Mask	
0080	7-Segment for POST	
0080 - 009F	DMA Page Register	(82371EB)
00A0 - 00BF	Interrupt Controller (Slave)	(82371EB)
00C0 - 00DF	DMA Controller (2)	(82371EB)
00F0•00FF	Co-Processor	
*190	7-segment LED for Test	
01F0 - 1F8	Hard Disk	(82371EB)
0279	IT8661F	
02E0 - 02EF	Reserve	
02E8 - 02EF	(COM4) Reserve	
02F8 - 2FF	Serial Port COM (2)	(IT8763F)
0300 - 031F	ETHERNET	(RTL8139B)
0320 - 032F	JS-170FR System Extension Port	
0378 - 037F	Parallel Port (1)	(IT8763F)
03B0 - 03DF	SVGA Controller	(SM710)
03E8 - 03EF	(COM3) Reserve	
03F0 - 03F7	Diskette Controller	(IT8763F)
03F8 - 3FF	Serial Port COM (1)	(IT8763F)
0A79	IT8661F	
0CF8 - 0CFF	430TX Chip Set	(82443BX)
3220 - 3227	Serial Port COM (3)	(PC16552DV)
3228 - 322F	Serial Port COM (4)	(PC16552DV)

Note: ETHERNET I/O Port Map Not Fixed.

Interrupt Level

Interrupt Level	Description	
SMI	(Power Management)	
NMI	I/O Check, Parity Error, Power Management	
IRQ 0	Timer Output	
IRQ 1	Keyboard Output Buffer Full	(IT8763F)
IRQ 2	8259 Slave Side Interrupt	
IRQ 3	Serial Port COM (2)	(IT8763F)
IRQ 4	Serial Port COM (1)	(IT8763F)
IRQ 5	Reserve	
IRQ 6	Diskette Controller	(IT8763F)
IRQ 7	Parallel Port1	(IT8763F)
IRQ 8	Real Time Clock	(82371EB)
IRQ10	Serial Port COM (4)	(PC16552DV)
IRQ11	Serial Port COM (3)	(PC16552DV)
IRQ12	Mouse	(IT8763F)
IRQ13	Co-processor	(CPU)
IRQ14	Hard Disk (Primary)	(IDE)
IRQ15	Hard Disk (Secondary)	(IDE)

Note : the jumper of the hardware should change The Interrupt of Power Management.
: ETHERNET Interrupt Level Not Fixed.

Pin assignments

Serial

COM1

9 pin D-SUB Male

No	IN/OUT	Signal
1	IN	CD
2	IN	RD
3	OUT	TD
4	OUT	DTR
5		GND
6	IN	DSR
7	OUT	RTS
8	IN	CTS
9	IN	RI

COM2

9 pin D-SUB Male

No	IN/OUT	Signal
1	IN	CD
2	IN	RD
3	OUT	TD
4	OUT	DTR
5		GND
6	IN	DSR
7	OUT	RTS
8	IN	CTS
9	IN	RI

COM3

8 pin Modular

No	IN/OUT	Signal
1		FG
2	OUT	RTS
3	IN	RD
4	IN	DSR or +5V or CD (Default)
5	OUT	TD
6	OUT	DTR
7		GND
8	IN	CTS (Default) or Not Connected

Cash Drawer

6 pin DIN Female

No	IN/OUT	Signal
1	OUT	Drawer_Open
2		GND
3	IN	Drawer_Status
4		GND
5	IN	Drawer Type
6		GND

Parallel

25 pin D-SUB Female

No	IN/OUT	Signal
1	IN/OUT	STROBE*
2	IN/OUT	Data Bit 0
3	IN/OUT	Data Bit 1
4	IN/OUT	Data Bit 2
5	IN/OUT	Data Bit 3
6	IN/OUT	Data Bit 4
7	IN/OUT	Data Bit 5
8	IN/OUT	Data Bit 6
9	IN/OUT	Data Bit 7
10	IN	ACK*
11	IN	BUSY
12	IN	PE
13	IN	SLCT
14	OUT	AUTO FD XT*
15	IN	ERROR*
16	OUT	INIT*
17	OUT	SLCT IN*
18		GND
19		GND
20		GND
21		GND
22		GND
23		GND
24		GND
25		GND

Video

15 pin D-SUB Female

No	IN/OUT	Signal
1	OUT	Video_Red
2	OUT	Video_Green
3	OUT	Video_Blue
4		NC
5		GND
6		Video GND(Red)
7		Video GND(Green)
8		Video GND(Blue)
9		NC
10		GND
11		NC
12	IN/OUT	SDA
13	OUT	H-Sync
14	OUT	V-Sync
15	IN/OUT	SCL

LAN

8 pin Modular (RJ-45)

No	IN/OUT	Signal
1	OUT	TX+
2	OUT	TX-
3	IN	RX+
4		NC
5		NC
6	IN	RX-
7		NC
8		NC

USB

USB Connector

No	IN/OUT	Signal
1, 5		+5V
2, 6	IN/OUT	USB_Data-
3, 7	IN/OUT	USB_Data+
4, 8		GND

Keyboard

6 pin mini DIN

No	IN/OUT	Signal
1	IN/OUT	Keyboard_Data
2	IN/OUT	Mouse_Data
3		GND
4		+5V
5	IN/OUT	Mouse_Clock
6	IN/OUT	Keyboard_Clock

Floppy Disk

26 pin mini I/O Connector

No	IN/OUT	Signal
1		GND
2	IN	INDEX*
3		+5V
4		DRV0
5		GND
6	IN	DCHG0*
7		NC
8		NC
9		NC
10		+5V
11	OUT	MTR0*
12	OUT	DIR
13		DENSEL
14	OUT	STEP*
15		GND
16	OUT	WDATA*
17		GND
18	OUT	WGATE*
19		GND
20	IN	TRK0*
21		GND
22	IN	WRPRT*
23	IN	RDATA*
24		GND
25	OUT	SIDESEL0
26		NC

PCI Interface

32bit Edge Connector, 5V system

No	B side	A side
1	-12V	TRST#
2	TCK	+12V
3	GND	TMS
4	TDO	TDI
5	+5V	+5V
6	+5V	INTA#
7	INTB#	INTC#
8	INTD#	+5V
9	PRSNT1#	Reserved
10	Reserved	+5V(I/O)
11	PRSNT2#	Reserved/SERIRQ
12	GND	GND
13	GND	GND
14	Reserved	Reserved
15	GND	RST#
16	CLK	+5V(I/O)
17	GND	GNT#
18	REQ#	GND
19	+5V(I/O)	Reserved/PME#
20	AD[31]	AD[30]
21	AD[29]	+3.3V
22	GND	AD[28]
23	AD[27]	AD[26]
24	AD[25]	GND
25	+3.3V	AD[24]
26	C/BE[3]#	IDSEL
27	AD[23]	+3.3V
28	GND	AD[22]
29	AD[21]	AD[20]
30	AD[19]	GND
31	+3.3V	AD[18]
32	AD[17]	AD[16]
33	C/BE[2]#	+3.3V
34	GND	FRAME#
35	IRDY#	GND
36	+3.3V	TRDY#
37	DEVSEL#	GND
38	GND	STOP#
39	LOCK#	+3.3V
40	PERR#	SDONE
41	+3.3V	SBO#

No	B side	A side
42	SERR#	GND
43	+3.3V	PAR
44	C/BE[1]#	AD[15]
45	AD[14]	+3.3V
46	GND	AD[13]
47	AD[12]	AD[11]
48	AD[10]	GND
49	GND	AD[09]
50	KEY	KEY
51	KEY	KEY
52	AD[08]	C/BE[0]#
53	AD[07]	+3.3V
54	+3.3V	AD[06]
55	AD[05]	AD[04]
56	AD[03]	GND
57	GND	AD[02]
58	AD[01]	AD[00]
59	+5V(I/O)	+5V(I/O)
60	ACK64#	REQ64#
61	+5V	+5V
62	+5V	+5V

IDE Interface

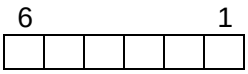
44pin Flat cable connector 2.0mm pitch

No	IN/OUT	Signal
1	IN	IDERST#
2		GND
3	IN/OUT	DATA7
4	IN/OUT	DATA8
5	IN/OUT	DATA6
6	IN/OUT	DATA9
7	IN/OUT	DATA5
8	IN/OUT	DATA10
9	IN/OUT	DATA4
10	IN/OUT	DATA11
11	IN/OUT	DATA3
12	IN/OUT	DATA12
13	IN/OUT	DATA2
14	IN/OUT	DATA13
15	IN/OUT	DATA1
16	IN/OUT	DATA14
17	IN/OUT	DATA0
18	IN/OUT	DATA15
19		GND
20		-

No	IN/OUT	Signal
21	OUT	DMARQ
22		GND
23	IN	IOW#
24		GND
25	IN	IOR#
26		GND
27	OUT	*IORDY
28	IN	CSEL
29	IN	DMACK#
30		GND
31	OUT	INTRQ
32		-
33	IN	DA1
34	IN	-(MASTER/SLAVE)
35	IN	DA0
36	IN	DA2
37	IN	CS1#
38	IN	CS3#
39	OUT	DASP#
40		GND
41		+5V
42		+5V
43		GND
44		-

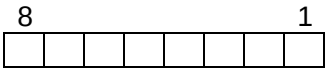
Dip Switches and Jumpers

Dip Switch 1



Bit	Explanation
1	Model identification bit On : 0 for I/O 324H bit5 Off : 1 for I/O 324H bit5 (Factory setting) Extended I/O port 324H bit 5 reflects to this setting.
2	Touch panel type On : Douwa (Carrol Touch) type (Factory setting for Germany Model only) Off : Fujitsu type (Factory Setting) Touch panel has two kinds of operating mode. Set this bit to Off (Fujitsu type) when you use Windows touch panel driver. For use with McDonald's application, set this bit to On (Douwa or Carrol Touch type).
3	Circuit for decoding (Magnetic card Swipe Reader : MSR) On : Circuit 2 (Formerly called as MAG2) (Factory setting) Off : Circuit 1 (Formerly called as MAG1) This model has two circuits (circuit 1 and 2) to decode data on magnetic stripe of card. Combination of a circuit and a track (a data stream on the magnetic stripe) is determined by dip switch 1 bit 5/6. (See below) When "Single" is set by dip switch 1 bit 4, only a circuit set by this bit is used for data decoding. When "Dual" is set by dip switch bit 4, both circuit 1 and 2 can be used to decode data. Bit 3 has no effect in this case.
4	Single and Dual circuit (Magnetic card Swipe Reader : MSR) On : Single (Factory setting) Off : Dual When this bit is set to "Single", the circuit selected by bit3 is used to decode data and application receives data of a track defined by bit 5/6 through the circuit. "Dual" setting uses both circuit 1 and 2 to decode data and application receives data of two tracks if both are on the card. Only data of existing track is returned to application even if this bit is set to "Dual".
6-5	Circuit and Track (Magnetic card Swipe Reader : MSR) bit6/5 is Off/Off : Circuit 1 expects JIS-II (Japan), circuit 2 expects ISO2 (JIS-I track2, Japan). bit6/5 is Off/On : Circuit 1 expects ISO1 (JIS-I track1, Japan), circuit 2 expects JIS-II. bit6/5 is On/Off : Circuit 1 expects ISO2, circuit 2 expects ISO1. bit6/5 is On/On : Circuit 1 expects ISO1, circuit 2 expects ISO2. Combination of these bits tells circuit to decode specified track data. For example circuit 1 decodes only ISO1 and circuit 2 decodes only ISO2 if bit 6/5 is On/On. If ISO2 data is input to circuit 1, it is treated as an error.

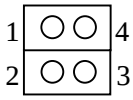
Dip Switch 2

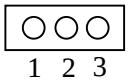


Bit	Explanation
1	Address control for extended I/O On : Software can enable/disable access to extended I/O ports. (Factory setting) Off : Extended I/O is always enabled. When this bit is set to On, software can enable/disable access to extended I/O ports (320H-32DH) by output data to 32FH. Setting this bit to Off always enables access to extended I/O. Software can't disable access to extended I/O through 32FH. System initializes hardware to disabling extended I/O if this bit is set to On. But BIOS setup finally determines initial state of accessibility, enable or disable.
2	Reserved for future Off : (Factory setting) Extended I/O 32DH bit5 reflects to this setting. This bit is reserved for future enhancements and any functions are not currently assigned to this bit.
4-3	Signal to open drawer bit4/3 is Off/Off : 217ms bit4/3 is Off/On : 145ms (Factory setting) bit4/3 is On/Off : 108ms bit4/3 is On/On : 72ms These bits define the period to activate signal for drawer open. Do not change these bits unless electrical specification of the drawer is modified in future.
5	Type of customer display On : Dual line type Off : One line type This bit is used to get type of customer display, one line type or dual. This bit actually reflects the status of dip switch 2 bit5. Setting this switch to OFF returns 1 to this bit. Extended port 32DH bit0 reflects to this bit. This bit should be set to indicate the customer display type actually connected if application program has a capability to adjust data for each display type.
6	Reserved for future Off : (Factory setting) Extended I/O 32DH bit1 reflects to this setting. This bit is reserved for future enhancements and any functions are not currently assigned to this bit.
8-7	Type of LCD bit7/6 is 11 : VGA (640x480) 10 : SVGA (800x600) 01 : XGA (1024x768) 00 : Reserved. Bit8/7 is Off/Off : VGA (640x480) (Factory setting) Bit8/7 is Off/On : SVGA (800x600) Bit8/7 is On/Off : XGA (1024x768) Bit8/7 is On/On : Reserved. Extended port 32DH bit6/7 reflects to these bits.

Jumper pins

Jumper numbers and pin numbers are printed on the main board. Direction of the jumpers follow the direction of printed numbers.





Pin	Explanation
JP1	VGAC 1-4 Short, 2-3 Short : 640x480 (Factory setting) 1-4 Short, 2-3 Open : 1024x768 1-4 Open, 2-3 Short : 800x600 1-4 Open, 2-3 Open : 1280x1024 This jumper sets the type of connected LCD to VGA controller.
JP2	Power fail interrupt 1-2 Short : NMI (Factory setting) 2-3 Short : SMI This jumper defines the type of interrupt by power fail.
JP3	COM3 IRQ 1-2 Short : IRQ11 (Factory setting) 2-3 Short : IRQ4 This jumper sets IRQ (interrupt) number used by COM3 UART.
JP4/5/6	Control signal of COM3 This jumper defines functions of some control lines on 8-pin modular connector of COM3. See table below for combination of pins.
JP7	CPU I/O voltage 1-2 Short : +2.5V (Factory setting) 2-3 Short : Reserved.
JP8	CPU GTL voltage Short : GTL=CORE voltage (Factory setting) Open : Reserved.
JP9	Power control Short : Boot by main power switch Open : Boot by front power switch (Factory setting)

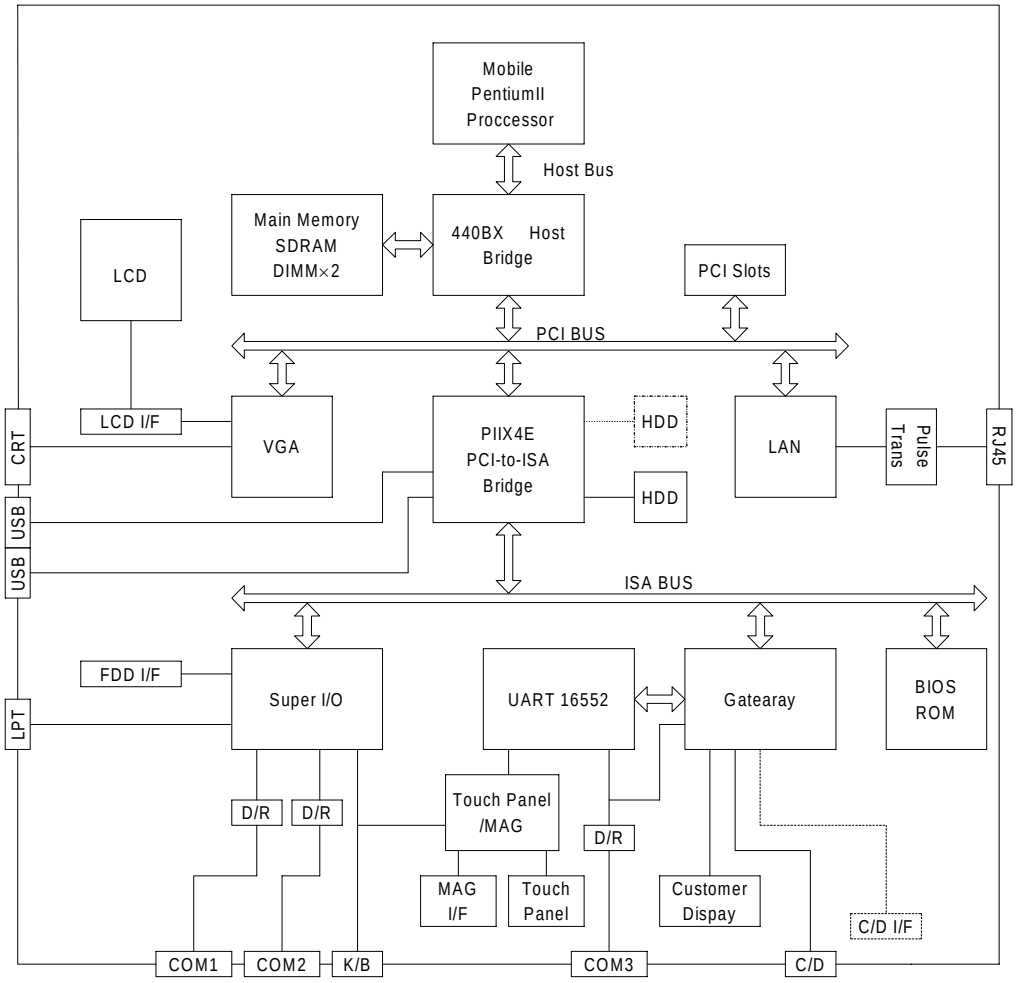
Signal on COM3 connector

JP4	Explanation
1-2 Short	Pin8 is CTS (Factory setting)
2-3 Short	Pin8 is Ground. CTS is always active.

JP5	JP6	Explanation
1-2 Short	2-3 Short	Pin4 is DCD. DSR is always active. (Factory setting)
2-3 Short	2-3 Short	Pin4 is DSR. DCD is always inactive.
1-2 Short	1-2 Short	Pin4 is fixed to +5V. DSR is always active and DCD is inactive.
2-3 Short	1-2 Short	Pin4 is fixed to +5V. DSR and DCD are always inactive.

2 Description of Operation

JS-170FR Block Diagram



Description of Main PCB Circuits

2.1.1 CPU PENTIUM-II 266MHz or 333MHz (Refer to the page 4-1.)

The CPU is operated at an operating clock signal frequency of 66MHz with the use of a mobile PENTIUM-II the core voltage of which is +1.6V.

Details of CPU operation are obtainable from the relevant catalog.

2.1.2 Chip set FW82443BX, FW82371EB (Refer to the page 4-1 and page 4-3.)

As a control chip set for CPU's peripheral circuits, two units in a pair of FW82443BX and FW82371EB are used.

The FW82443BX is directly combined with the CPU, and it is mainly in charge of memory control and PCI bus control.

In order to realize the AT compatibility, the FW82371EB is internally equipped with the basic LSI and the control circuit that functions as a bridge circuit between the PCI bus and the ISA bus.

When the power supply is ON, the FW82443BX is used to execute initializing setting for the hardware with the aid of the memory address bus (MAB 6# ~ 12#).

For other details, refer to the relevant catalogs.

	FUNCTION	
MAB6#	Buffer Mode	1 : Mobile 0 : Desktop
MAB7#	MM Config	1 : Tri-stste 0 : Normal
MAB9#	AGP	1 : Disable 0 : Enable
MAB10#	Quick Start	1 : Quick Start 0 : Stop Clock
MAB11#	Queue Depth	1 : 4 0 : 1
MAB12#	CLOCK	1 : 100MHz 0 : 66MHz

2.1.2.1 FW82371EB Pin Assignment

Pin No.	Signal name	IN/OUT	Functions
Y 04	AEN	OUT	The signal used to indicate that the DMA cycle is currently executed. Active :High
M 20	A20M#	OUT	The signal intended to make the system address line A20 stay in internal mask off state. (→CPU)
P 01	A20GATE	IN	The gate signal for the address line A20. (←KBC)
B 01	AD31	IN/OUT	PCI system address data bus.
C 01	AD30		
E 01	AD29		
D 01	AD28		
A 02	AD27		
B 02	AD26		
C 02	AD25		
E 02	AD24		
B 03	AD23		
C 03	AD22		
E 03	AD21		
D 03	AD20		
A 04	AD19		
B 04	AD18		
C 04	AD17		
E 04	AD16		
E 06	AD15		
D 06	AD14		
A 07	AD13		
B 07	AD12		
C 07	AD11		
D 07	AD10		
A 08	AD9		
B 08	AD8		
E 08	AD7		
D 08	AD6		
A 09	AD5		
B 09	AD4		
C 09	AD3		
D 09	AD2		
A 10	AD1		
B 10	AD0		
J 17	APICACK#	OUT	APIC Acknowledge signal to APICREQ#.
H 18	APICCS#	OUT	APIC chip select signal.
K 18	APICREQ#	IN	APIC bus request signal.
U 10	BALE	OUT	Address latch enable signal.
M 02	BIOSCS#	OUT	ROM's chip select signal for BIOS. Active : Low
U 19	BATLOW#/GPI9	IN	Used as a general-purpose input port.
C 08	C/BE0#	IN/OUT	PCI command/byte enable signal. Active : Low
C 06	C/BE1#		
D 04	C/BE2#		
D 02	C/BE3#		
L 03	CLK48	IN	Clock input for USB. Fixed at 48MHz.
C 10	CLKRUN#	IN/OUT	PCI bus Clock control signal.
R 17	CONFIG1	IN	Configuration CONF I G1=Low←PENTIUM, High←PENTUM Pro
R 18	CONFIG2		CONF I G2=Reserve
M 19	CPURST	OUT	Reset signal to CPU. Active : High
R 01	CPU_STP#	OUT	Stop signal to CPU clock (→ Clock synthesizer) Active : Low
E 05	DEVSEL#	IN/OUT	Device select signal. Active : Low

Pin No.	Signal name	IN/OUT	Functions
U 14 W 06 Y 10 V 05 T 15 V 16 W 17	DACK0# DACK1# DACK2# DACK3# DACK5# DACK6# DACK7#	OUT	ACK signal to DRQ. Active : Low
W 15 U 06 V 02 U 05 Y 16 U 16 U 17	DRQ0 DRQ1 DRQ2 DRQ3 DRQ5 DRQ6 DRQ7	IN	DMA transfer request signal. Active : High
V 20	EXTSMI#	IN/OUT	External system management interrupt.
E 06	FRAME#	IN/OUT	PCI bus The signal to indicate that the bus cycle is currently executed. Active : Low
K 19	FERR#	IN	Floating decimal point error signal. Active : Low
N 01 P 02 P 04	GNTA# GNTB# GNTC#	OUT	PCI bus DMA enable signal. Active : Low
P 19 L 02 J 03 L 05 K 03 K 04 H 01 H 04 H 05 G 03	GPI1 GPI13 GPI14 GPI15 GPI16 GPI17 GPI18 GPI19 GPI20 GPI21	IN	Used as a general-purpose input port.
G 04 T 19 G 05 F 02 F 03 F 04	GP00 GP08 GP027 GP028 GP029/IRQ9_0 GP030	OUT	Used as a general-purpose input port.
A 03	IDSEL	IN	PCI The signal used to specify the target device.
L 19	INTR	OUT	Interrupt request signal. IRQ0-IRQ15 (→CPU) Active : High
L 17	IGNNE#	OUT	Output to disregard the floating decimal point error. (→CPU)
L 18	INIT	OUT	The initialize request signal to the CPU. (→CPU) Active : High
V 12	IOCS16#	IN	ISA Used to specify the data bus width of I/O. Low → 16-bit, High → 8-bit.
Y 01	IOCHK#/GPI0	IN	ISA The signal to indicate that a correction impossible error has occurred. (→NMI) Active : Low
T 03	IOCHRDY	IN	ISA Used when the bus cycle is extended. (Wait signal) Active : Low
T 04	IOW#	IN/OUT	ISA Write signal to the I/O device. Active : Low
Y 05	IOR#	IN/OUT	ISA Read signal to the I/O device. Active : Low
B 05	IRDY#	IN/OUT	PCI The signal to indicate that the initiator is enabled to transfer data.

Pin No.	Signal name	IN/OUT	Functions	
H 20	IRQ0	OUT	System timer interrupt signal being output.	
J 20	IRQ1	IN	Mask enabled interrupt request signal. (← Keyboard controller)	Active : High
T 09	IRQ3	IN	Mask enabled interrupt request signal. (← Serial port 2)	Active : High
W 09	IRQ4	IN	Mask enabled interrupt request signal. (← Serial port 1)	Active : High
U 08	IRQ5	IN	Mask enabled interrupt request signal.	Active : High
V 08	IRQ6	IN	Mask enabled interrupt request signal. (← FDC)	Active : High
Y 08	IRQ7	IN	Mask enabled interrupt request signal. (← Parallel port 1)	Active : High
Y 20	IRQ8#/GPI6	IN/OUT	Mask enabled interrupt request signal. (← For RTC)	Active : Low
U 01	IRQ9	IN	Mask enabled interrupt request signal. (← ETHERNET)	Active : High
U 12	IRQ10	IN	Mask enabled interrupt request signal. (← Serial port 4)	Active : High
W 13	IRQ11	IN	Mask enabled interrupt request signal. (← Serial port 3)	Active : High
T 13	IRQ12/M	IN	Mask enabled interrupt request signal. (← PS/2 mouse)	Active : High
V 14	IRQ14	IN	Mask enabled interrupt request signal. (← E-IDE)	Active : High
Y 14	IRQ15	IN	Mask enabled interrupt request signal.	Active : High
K 01	KBCCS#/GPO26	OUT	Chip select signal to the keyboard controller.	Active : Low
Y 15 T 14 W 14 U 13 V 13 Y 13 T 12	LA17 LA18 LA19 LA20 LA21 LA22 LA23	IN/OUT	ISA An address bus not latched yet.	
N 04	MCCS#	OUT	I/O An output that is active with I/O address 62h and 66h.	Active : Low
Y 12	MEMCS16#	IN	ISA Used to specify the data bus width of the memory. Low → 16-bit, High → 8-bit.	
V 15	MEMR#	IN/OUT	ISA The read signal to the memory device. (All area)	Active : Low
U 15	MEMW#	IN/OUT	ISA The write signal to the memory device. (All area)	Active : Low
L 20	NMI	OUT	Non-maskable interrupt lower than SMI#. (→ CPU)	
J 01 J 02	OC0# OC1#	IN	Overcurrent detector pin of the USB port.	
V 11	OSC	IN	Clock input for timer counter (8254). Fixed at 14.3181MHz.	
B 06	PAR	OUT	PCI PCI Bus parity signal.	
D 11	PCICLK	IN	PCI Clock signal for the PCI bus. 33MHz/30MHz	
E 10 A 11 B 11 C 11	PCIREQA# PCIREQB# PCIREQC# PCIREQD#	IN	PCI Bus request signal.	Active : Low
A 01	PCIRST#	OUT	PCI Asynchronous reset signal.	Active : Low
R 02	PCI_STP#	OUT	Clock stop request signal for PCI. (→ Clock synthesizer)	Active : Low
L 04 N 05	PCS0# PCS1#	OUT	Programmable chip select signal.	Active : Low
G 16 G 18 G 17	PDA0 PDA1 PDA2	OUT	E-IDE Primary side address.	
H 17	PDCS1#	OUT	The signal that is active with I/O address 01F0-01F7h of E-IDE.	Active : Low
H 16	PDCS3#	OUT	The signal that is active with I/O address 03F6-03F6h of E-IDE.	Active : Low
F 20 E 18 E 20 D 18 D 20 C 20 B 20 A 20	PDD0 PDD1 PDD2 PDD3 PDD4 PDD5 PDD6 PDD7	IN/OUT	E-IDE Primary data bus.	

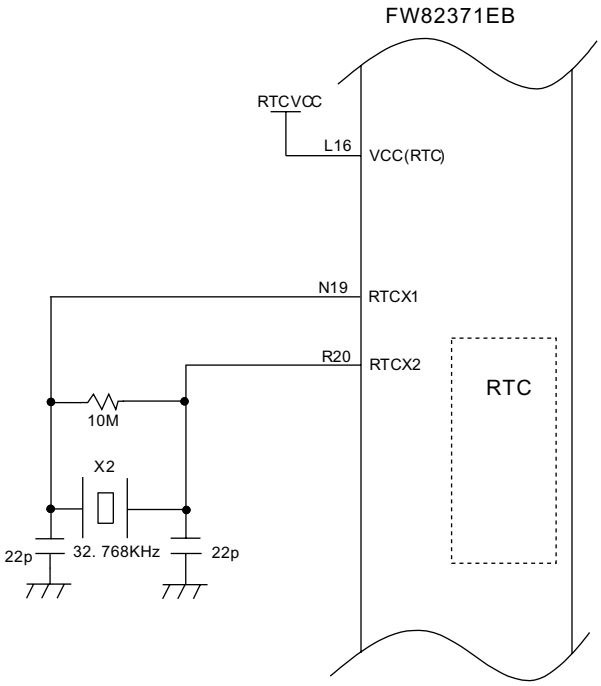
Pin No.	Signal name	IN/OUT	Functions
A 19 B 19 C 19 D 19 D 17 E 19 E 17 F 19	PDD8 PDD9 PDD10 PDD11 PDD12 PDD13 PDD14 PDD15	IN/OUT	E-IDE Primary data bus.
G 19	PDDACK#	OUT	E-IDE Acknowledge to primary side PDDREQ.
F 18	PDDREQ	IN	E-IDE Primary side DMA request signal.
F 17	PDIOR#	OUT	E-IDE Primary side read signal.
F 16	PDIOW#	OUT	E-IDE Primary side write signal.
G 20	PIORDY	IN	E-IDE Primary side ready signal.
B 12	PHLD#	OUT	PCI bus hold request signal.
A 12	PHLDA#	IN	PCI Hold acknowledge signal to PHLD#.
R 03 R 04 P 05 G 01	PIRQA# PIRQB# PIRQC# PIRQD#	IN/OUT	OCI bus interrupt signal.
U 20	PWRBTN#	IN	Input pin for system's ON/OFF.
M 18	PWROK	IN	System power input signal. Active : High
N 20	RCIN#	IN	Initialize request signal to the CPU. (← KBC)
P 18	RI#/GPI12	IN	Used as a general-purpose input port.
M 17	RSMRST#	IN	An input intended to reset the internal suspension state. Active : Low
L 01 K 02	RTCALE/GP025 RTCCS#/GP024	OUT	Used as a general-purpose output port.
N 19 R 20	RTCX1 RTCX2	IN/OUT	Clock signal of 32.768kHz for RTC.
W 07	REFRESH#	IN/OUT	Memory refresh signal to the ISA bus. Active : Low
M 01 N 02 P 03	REQA#/GPI2 REQB#/GPI3 REQC#/GPI4	IN	DMA request signal for the PCI bus. Active : Low
W 01	RSTDRV	OUT	Reset signal for the ISA system logic. Active : High
U 11 T 11 W 11 Y 11 T 10 W 10 U 09 V 09 Y 09 T 08 W 08 U 07 V 07 Y 07 V 06 Y 06 T 05 W 05 U 04 V 04	SA0 SA1 SA2 SA3 SA4 SA5 SA6 SA7 SA8 SA9 SA10 SA11 SA12 SA13 SA14 SA15 SA16 SA17 SA18 SA19	IN/OUT	ISA System address bus.

Pin No.	Signal name	IN/OUT	Functions
V 03 W 03 U 02 T 02 W 02 Y 02 T 01 V 01 W 16 T 16 Y 17 V 17 Y 18 W 18 Y 19 W 19	SD0 SD1 SD2 SD3 SD4 SD5 SD6 SD7 SD8 SD9 SD10 SD11 SD12 SD13 SD14 SD15	IN/OUT	ISA system data bus.
W 12	SBHE#	IN/OUT	Used to indicate that SD8-SD15 of the ISA transfer data are effective. Active : Low
B 18	SDCS1#	OUT	The signal that becomes active with E-IDE's second I/O address 0170-0177h. Active : Low
C 18	SDCS3#	OUT	The signal that becomes active with E-IDE's second I/O address. Active : Low
E 15 B 15 D 14 C 14 A 14 C 13 A 13 C 12 D 12 B 13 D 13 B 14 E 14 A 15 C 15 D 15	SDD0 SDD1 SDD2 SDD3 SDD4 SDD5 SDD6 SDD7 SDD8 SDD9 SDD10 SDD11 SDD12 SDD13 SDD14 SDD15	IN/OUT	E-IDE Secondary data bus.
C 17 B 17 A 18	SDA0 SDA1 SDA2	OUT	E-IDE Secondary side address.
A 17	SDDACK#	OUT	E-IDE Acknowledge to secondary side PDDREQ.
A 16	SDDREQ	IN	E-IDE Secondary side DMA request signal.
C 16	SDIOR#	OUT	E-IDE Secondary side read signal.
B 16	SDIOW#	OUT	E-IDE Secondary side write signal.
D 16	SIORDY	IN	E-IDE Secondary side ready signal.
A 06	SERR#	IN/OUT	PCI system error signal. Active : Low
J 19	SERIRQ/GPI7	IN/OUT	Serial bus interrupt signal.
K 20	SLP#	OUT	Sleep request signal to the PENTIUM II. Active : Low
N 17	SMBALERT#	IN	Interrupt signal for the system management bus.
R 19	SMBCLK	IN/OUT	Clock signal for the system management bus.
T 20	SMBDATA	IN/OUT	Serial data for the system management bus.
U 03	SMEMW#	IN/OUT	Write signal to the ISA 0-1Mbyte memory device. Active : Low
W 04	SMEMR#	IN/OUT	Read signal to the ISA 0-1Mbyte memory device. Active : Low
P 20	SMI#	OUT	Higher preference non-maskable interrupt. (→ CPU) Active : Low
K 17	SPKR	OUT	Speaker output pin.
D 05	STOP#	IN/OUT	PCI Request signal from the target to the initiator for the suspension of execution. Active : Low
J 18	STPCLK#	OUT	The signal used to specify the suspension of clock supply to CPU's internal core. (→ CPU)

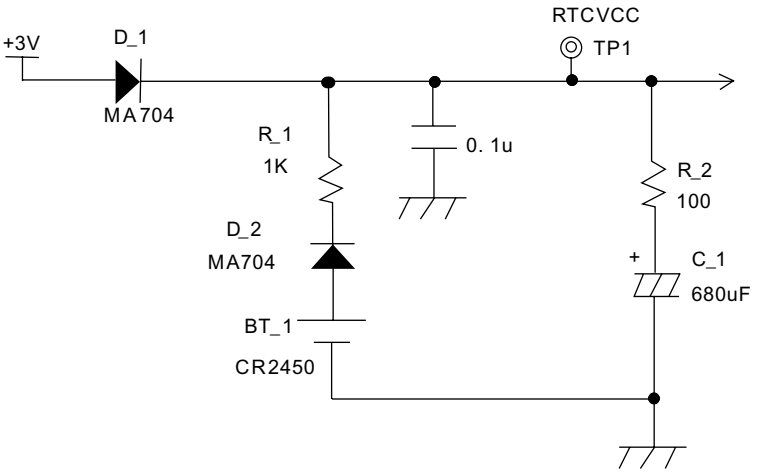
Pin No.	Signal name	IN/OUT	Functions
W 20 V 19 U 18	SUSA# SUSB# SUSC#	OUT	Device power supply control signal.
P 17	SUSCLK	OUT	Suspension clock. 32.768kHz
T 17 T 18	SUSSTAT1# SUSSTAT2#	OUT	Suspension status output signal.
T 07	SYSCLK	OUT	ISA bus system clock
V 10	TC	OUT	Pulse signal to be output when the terminal count of the DMA channel is attained. Active : High
V 18	TEST#	IN	Test pin.
H 19	THRM#/GPI8	IN	Temperature sensing signal input pin.
C 05	TRDY#	IN/OUT	The signal used to indicate that the PCI target is enabled for data transfer.
G 02 H 03	USBP0+ USBP0-	IN/OUT	Serial bus for USB Port 0.
F 01 H 02	USBP1+ USBP1-	IN/OUT	Serial bus for USB Port 1.
M 03	XDIR#	OUT	X-bus data transceiver's direction control signal. High : For write, Low : For read.
M 04	XOE#	OUT	X-bus output enable control signal. Active : Low
Y 03	ZEROWS#	IN	ISA The signal to indicate that the currently executed bus cycle can be finished without the wait state.
K 16	ZZ	OUT	L2 CACHE control signal.

2.1.2.2 RTC (Real Time Clock) circuit

The FW82371EB incorporates an RTC function.
The RTC includes the hardware for clock and calendar functions and the battery backup type CMOS-RAM that can manage the hardware setup information.
Operation is compatible with the MC146818.
To actuate the RTC, it is necessary to install the battery and the oscillator externally.
The oscillatory frequency is 32.768kHz, fixed. The clock is also of the backup type.

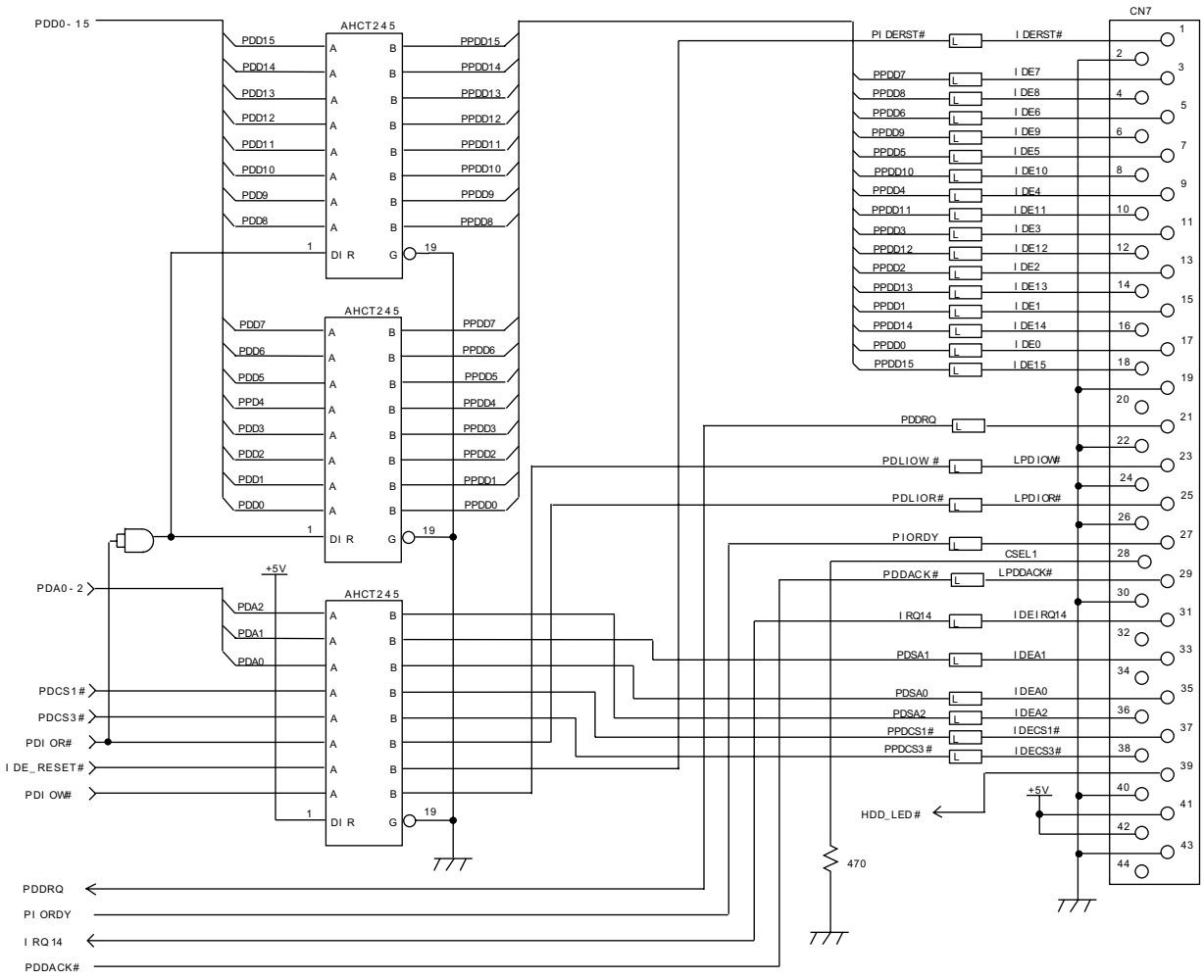


This system uses a lithium battery to back up the RTC circuit.
The battery (BT_1) is a charge-disabled coin type primary battery that maintain a voltage of about +3.0V.
When the power supply is ON, +3V (+3.3V) is turned to the RTCVCC voltage via D_1. When the power supply is OFF, the battery voltage is used as the RTCVCC voltage via D_2.
The C_1 capacitor is a backup capacitor to be used during the replacement of battery.
The battery backup time is only about 2 minutes, and therefore care must be taken at the time of replacement.



2.1.2.3 IDE interface

The E-IDE (Enhanced IDE) interface circuit for hard disc is incorporated in the FW82371EB.
The E-IDE is provided with two interfaces, Primary and Secondary.
Since the E-IDE interface is intended to be exclusively used for AT-compatible machines and a control circuit is accommodated on the HDD side, it is connected with the parallel data bus with the use of control signals.
With an I/O access action from the CPU side, the E-IDE interface performs direct access to the register group in the drive in order to control this drive. The primary side drive is selected by PDA0~PDA2 and the chip select PDCS1# and PDCS3#1. The read and write functions are selected by the use of the PDIOW# and PDIOR# signals.
For interrupt, IRQ14 is used on the primary side and IRQ15 is used on the secondary side.

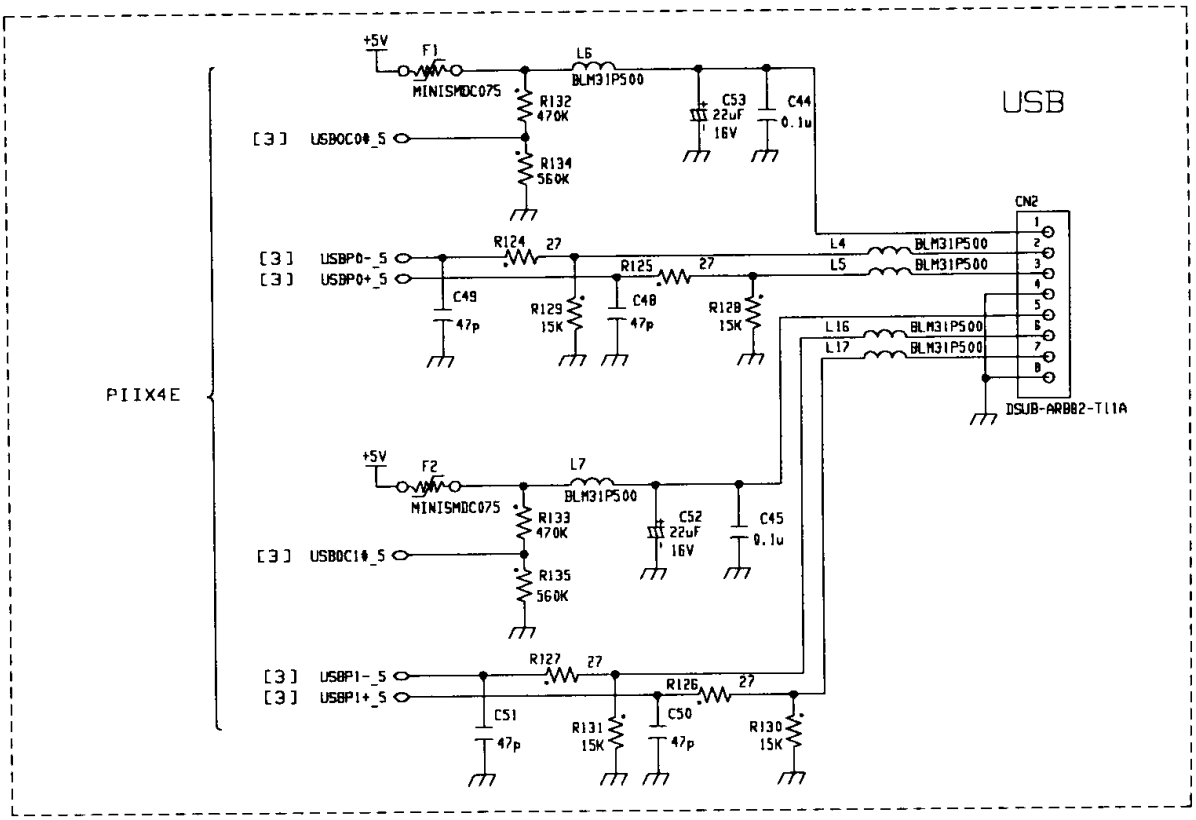


PDCS1#	PDCS3#	PDA2	PDA1	PDA0	PDIOR# = "L"	PDIOW# = "L"
L	L	X	X	X	Disabled	Disabled
L	H	L	L	L	Data register	Data register
L	H	L	L	H	Error registe	Future register
L	H	L	H	L	Selector counter	Selector counter
L	H	L	H	H	Sector number	Sector number
L	H	H	L	L	Cylinder low	Cylinder low
L	H	H	L	H	Cylinder high	Cylinder high
L	H	H	H	L	Drive/ head	Drive/ head
L	H	H	H	H	Status	Command
H	L	L	X	X	High impedance	High impedance
H	L	H	L	X	High impedance	High impedance
H	L	H	H	L	Alternate status	Device control
H	L	H	H	H	Drive address	Not used
H	H	X	X	X	High impedance	High impedance

Address map of E-IDE register

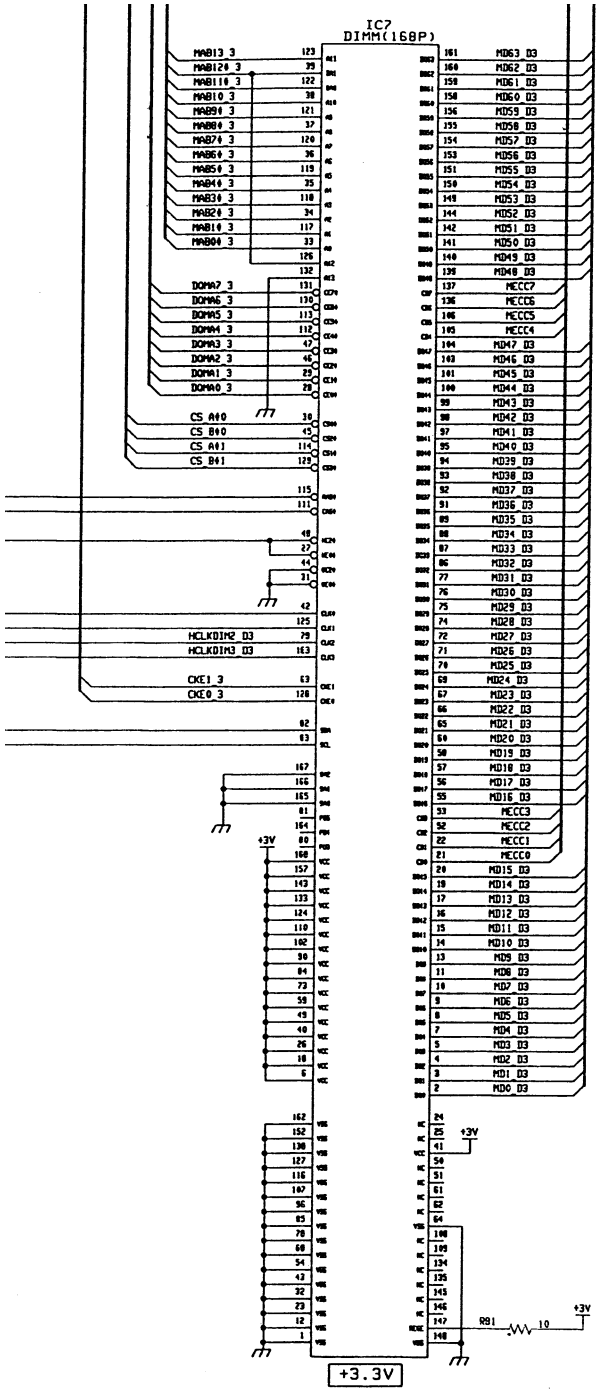
2.1.2.4 USB interface

This system is provided with two circuits of the USB (Universal Serial Bus) interfaces.
The power supply fed to the USB connector is a +5V power source that feeds a current at a maximum of 0.75A.
The USB controller is located in the FW82371EB of the chip set. The basic operation clock is maintained at 48MHz.
The USB port can be connected with the keyboard, mouse, modem, printer, etc. When a hub is externally connected, multiple connections can be made at the same time.



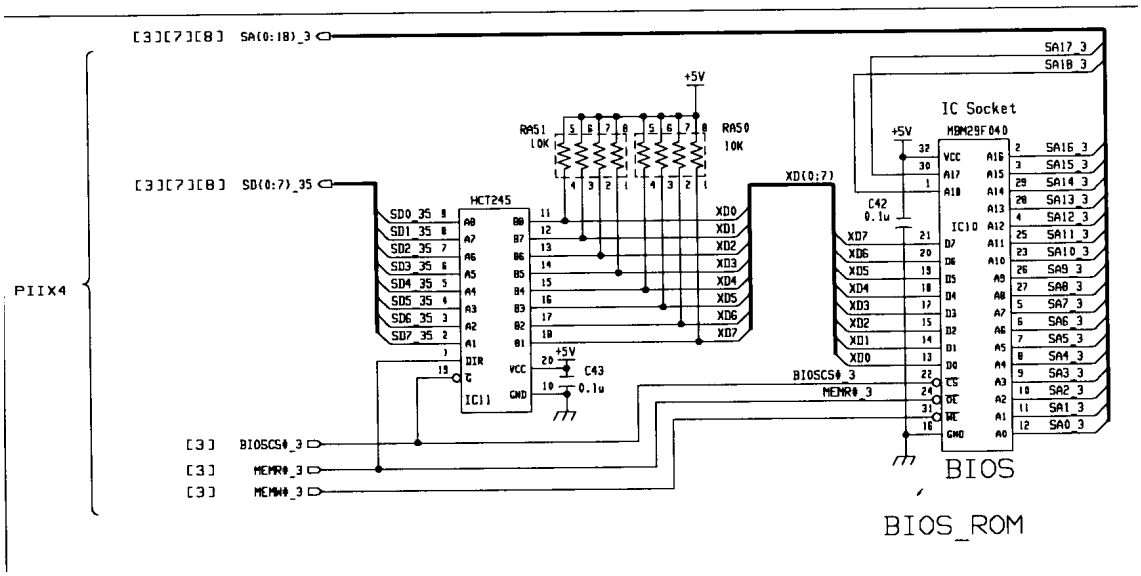
2.1.3 Main RAM circuit

A 3.3V DIMM (168-pin) is used for the main RAM of this system.
The DIMM can mount an SDRAM or EDO type memory and the installed capacity is controlled by the software. The circuit provided with the ECC parity is also available.
The maximum capacity of a single DIMM is 128Mbytes. Therefore, it is possible to increase the capacity up to 256Mbytes if two chips are used.
Both SDRAM and EDO can be mounted in mixture. There is no discrimination in mounting positions.
For the EDO, refreshment is controlled by the FW82443BX. At every period of about 15µsec., refreshment is carried out by the CAS before RAS system.
The speed used for the EDO is 60nsec. max., and 10nsec. max. for the SDRAM.



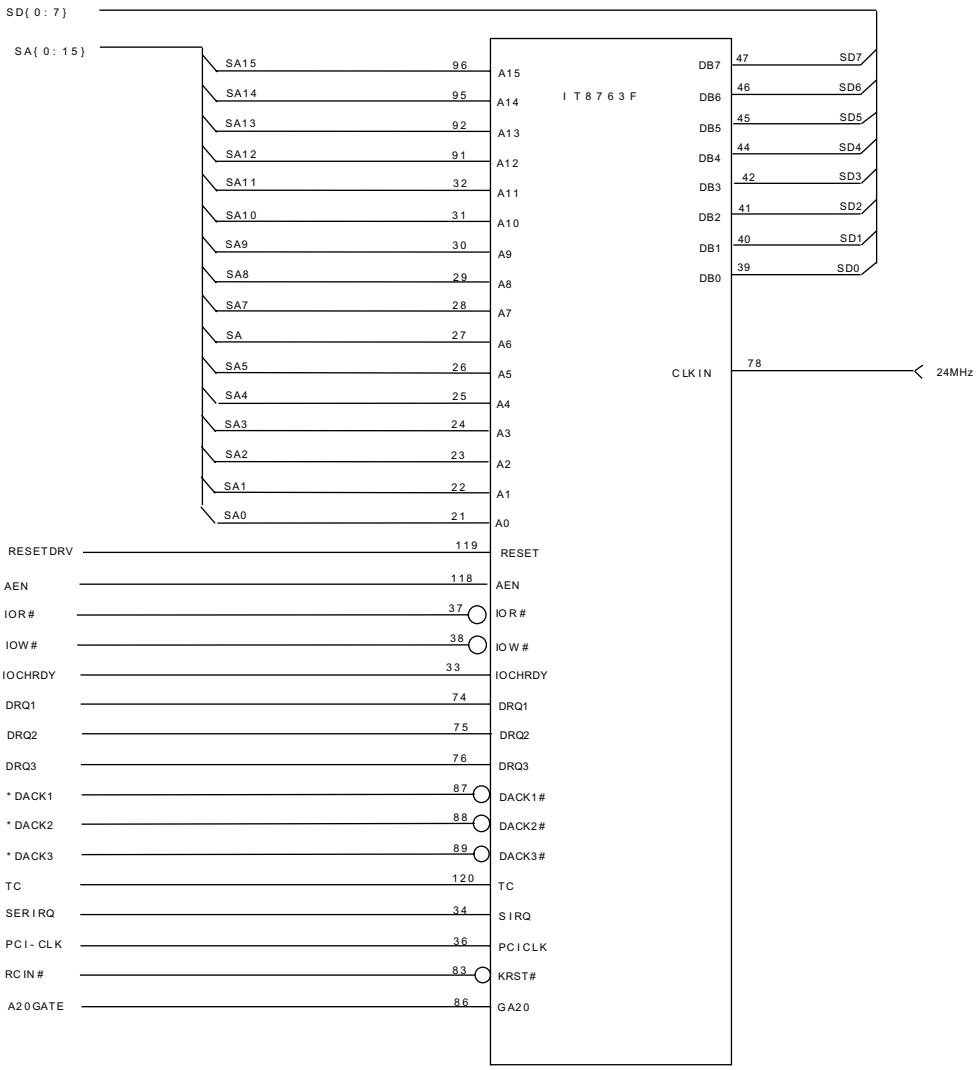
2.1.4 BIOS ROM

A flash memory of 512K × 8 bits is used for the BIOS.
ROM's address decoding is undertaken by the chip set. The BIOS setting area is 000E0000h ~ 000FFFFFh or FFFE0000h ~ FFFFFFFFh that is the most significant area for the CPU. (Either address can be accessed.)
When used as a 512K type, continuous access becomes possible in the virtual memory area.
The flash memory is a write-enabled memory that requires command control by software when writing.
The BIOS ROM data bus is connected to the X bus since ROM's fan-out is small. It is then connected to the system data bus (SD bus) via the buffer (HCT245).
Since this system uses the shadow memory method, the contents of ROM are written in the main memory when the BIOS is started. After the system has been started, the CPU disconnects the ROM and works with the RAM.
The shadow memory method is effective to raise the processing speed by performing system's operation with the RAM the access speed of which is higher than that of the ROM. It is possible to separate the programs that are not required in other cases than system start. As a result, the work area can be expanded.



2.1.5 IT8673F circuit

The IT8673F is used as an LSI for the control of peripheral I/O circuits, keyboard, and mouse.
The IT8673F functions as the two UART units (equivalent to 16C550), the parallel port with the FDC (equivalent to DP8473) incorporating the analog data separator, and the #8042 compatible keyboard controller having the mouse control function conforming to the PS/2 Specification.
An I/O address decoder circuit conforming to the Plug & Play Specification V1.0a is incorporated to realize AT compatible functions.
The respective functions are set up with the software.



2.1.5.1 IT8673F Pin Assignment

Pin No.	Signal name	IN/OUT	Functions
5	DENSEL#	OUT (*)	FDD packing density select signal. High•500K/1Mbps ,Low•250K/300Kbps
6	MTR0#	OUT(*)	Motor enable signal to the FDD Drive 0. Active : Low
7	DRV1#	OUT(*)	Select signal to the FDD Drive 1. Active : Low
8	DRV0#	OUT(*)	Select signal to the FDD Drive 0. Active : Low
9	MTR1#	OUT(*)	Motor enable signal to the FDD Drive 1. Active : Low
11	FDDIR	OUT(*)	The signal to specify the direction of the FDD head movement. Low → Step in, High → Step out.
12	STEP#	OUT(*)	The signal to move the head during FDD seek. Active : Low
13	WDATA#	OUT(*)	FDD write data signal. Active : Low
14	WGATE#	OUT(*)	Write circuit enable signal for the drive that has seized the FDD. Active : Low
15	HDSEL	OUT(*)	FDD head select signal. Low → Head 1, High → Head 0.
16	INDEX#	IN	The signal to indicate the first FDD track. Active : Low
17	TRK0#	IN	Position signal for FDD Track 0. Active : Low
18	WPRT#	IN	FDD write protect (write disable) signal. Active : Low
19	RDATA#	IN	FDD read signal.
20	DSKCHG	IN	The signal used to indicate that the FDD drive door is open. Active : High
21 | 32 91 92	A0 | A11 A12 A13	IN	System address bus. Address-latched signal.
33	IOCHRDY	OUT(*)	The signal that turns low when I/O address 210H is accessed.
34	SIRQ	IN/OUT	Serial interrupt signal.
36	PCICLK	IN	PCI clock for SIRQ sync.
37	IOR#	IN	Read signal to the I/O device. Active : Low
38	IOW#	IN	Write signal to the I/O device. Active : Low
39 | 42 44 | 47	D0 | D3 D4 | D7	IN/OUT	System data bus.
48	RXD1	IN	COM1 serial input data.
49	TXD1	OUT	COM1 serial output data.
50	DSR1#	IN	COM1 data set ready signal. Active : Low
51	RTS1#/PIN95SEL	IN/OUT	COM1 send request signal. Active : Low Used at the high level with pin 95 for SA14 when the power supply is ON.
52	CTS1#	IN	COM1 send enable signal. Active : Low
53	DTR1#/PIN96SEL	OUT	COM1 data terminal ready signal. Active : Low Used at the high level with pin 96 for SA15 when the power supply is ON.
54	RI1#	IN	COM1 ring indicator signal. Active : Low
55	DCD1#	IN	COM1 data carrier detect signal. Active : Low
56	RI2#	IN	COM2 ring indicator signal. Active : Low
57	DCD2#	IN	COM2 data carrier detect signal. Active : Low
58	RXD2	IN	COM2 serial input data.
59	TXD2	OUT	COM2 serial output data.
60	DSR2#	IN	COM2 data set ready signal. Active : Low
61	RTS2#/KBC_IROM	OUT	COM2 send request signal. Active : Low Used at the high level with the KB controller's built-in ROM when the power supply is ON.
62	CTS2#	IN	COM2 send enable signal. Active : Low Used to enable the KB controller at the high level when the power supply is ON.
63	DTR2#/KBCEN	OUT	COM2 data terminal ready signal. Active : Low

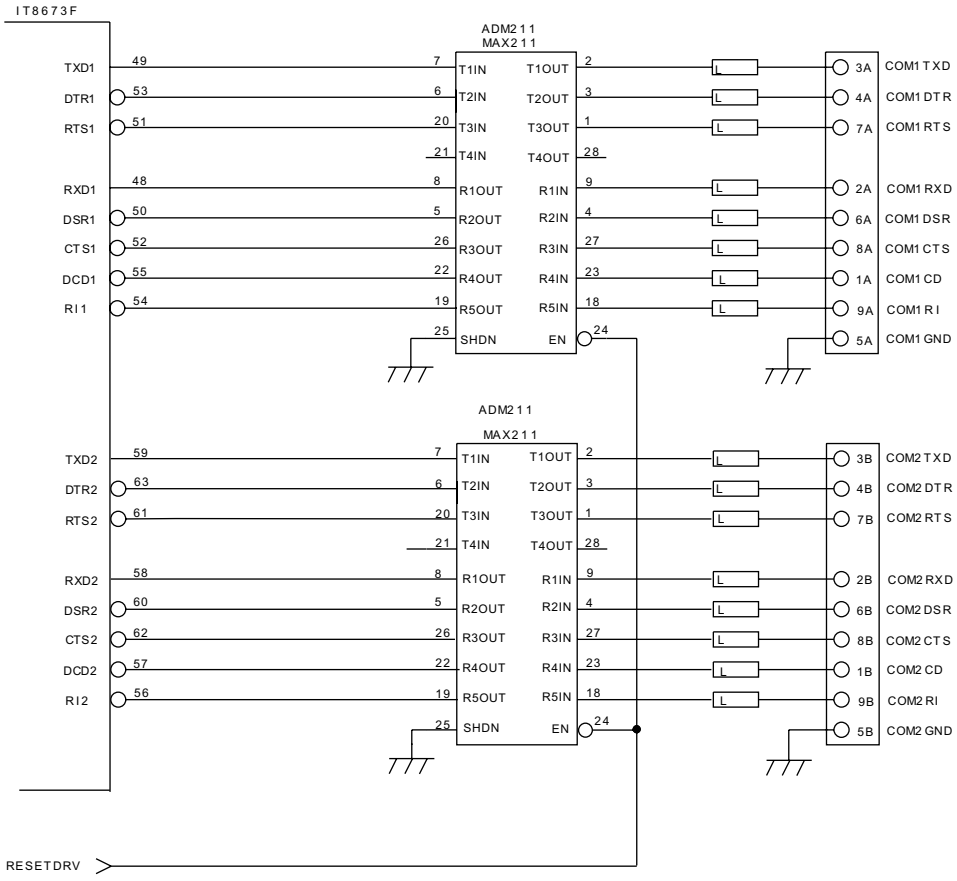
Pin No.	Signal name	IN/OUT	Functions
64	FAN_TAC1	IN	FAN rpm input pin.
65	FAN_CTL1	OUT	FAN control signal.
66 68 | 71	GP10 GP17 | GP14	IN/OUT	General-purpose I/O port pin.
72	FAN_CTL2/GP13	IN/OUT	FAN control signal.
73	FAN_TAC2/GP12	IN/OUT	FAN rpm input pin.
74 75 76	DRQ1 DRQ2 DRQ3	OUT	DMA request signal. Active : High
78	CLKIN	IN	External 24MHz clock input pin.
79	KDAT	IN/OUT	Keyboard Data
80	KCLK	IN/OUT	Keyboard CLOCK
81	MDAT	IN/OUT	PS/2 Mouse Data
82	MCLK	IN/OUT	PS/2 Mouse CLOCK
83	KRST#	OUT	Infrared serial receive data pin. Active : Low
84	IRRX	IN	Infrared serial receive data pin.
85	IRTX	OUT	Infrared serial transmit data pin.
86	GA20	OUT	Gate address 20
87 88 89	DACK1# DACK2# DACK3#	IN	DMA acknowledge signal. Active : Low
90	PSON/GP11	IN/OUT	Output for Power ON. Active : Low General-purpose I/O port.
93	PWRON#/PME#	IN/OUT	Power ON switch output.
94	PANSWH#	IN	Panel switch input pin. Active : Low
95	SA14/FAN_TAC3	IN	System address bus 14 Address-latched signal.
96	SA15/FAN_CTL3	IN/OUT	System address bus 15 Address-latched signal.
98	COPEN#	OUT	Case open sensor output. Active : Low
100	SLCT	IN	Select signal to be turned high by the selected printer.
101	PE	IN	Paper empty input signal. High → No paper remaining.
102	BUSY	IN	Busy signal sent from the printer. Used to indicate that the printer cannot accept data. Active : High
103	ACK#	IN	Acknowledge signal sent from the printer. Used to indicate that the printer has accepted data. Active : Low
105 | 112	PD7 | PD0	IN/OUT	Parallel port data.
113	SLIN*	OUT(*)	Printer select signal. Active : Low
114	INIT*	OUT(*)	Printer's initial setting signal. Active : Low
115	ERR#	IN	Error signal sent from the printer. Active : Low
116	AFD#	OUT(*)	Printer's automatic carriage return signal. Active : Low
117	STB#	OUT(*)	The signal to indicate that the parallel port data are effective. Active : Low
118	AEN	IN	Address enable signal. Normal: High, DMA: Low.
119	RESET	IN	Hardware reset signal. Active : High
120	TC	IN	The signal to indicate that DMA data transfer has been over. Active : High

Note) The OUT signals marked by the asterisk (*) are the open drain output signals.

2.1.5.2 Serial port (COM1, 2)

The IT8673 incorporates the two 16C550 compatible serial port controllers (UART1 and UART2).
The 24MHz signal (fixed) is 13-frequency-divided into 1.8462MHz that is then used to produce a Baud rate clock. This port operates in an asynchronous mode.
The two controllers are independent of each other. By setting up a configuration port with software, address and interrupt assignment can be carried out.
The basic setting for this system is as specified below.

IT8673F	System	I/O address	Interrupt level
UART1	COM1	3F8h-3FFh	IRQ4
UART2	COM2	OUT	IRQ3



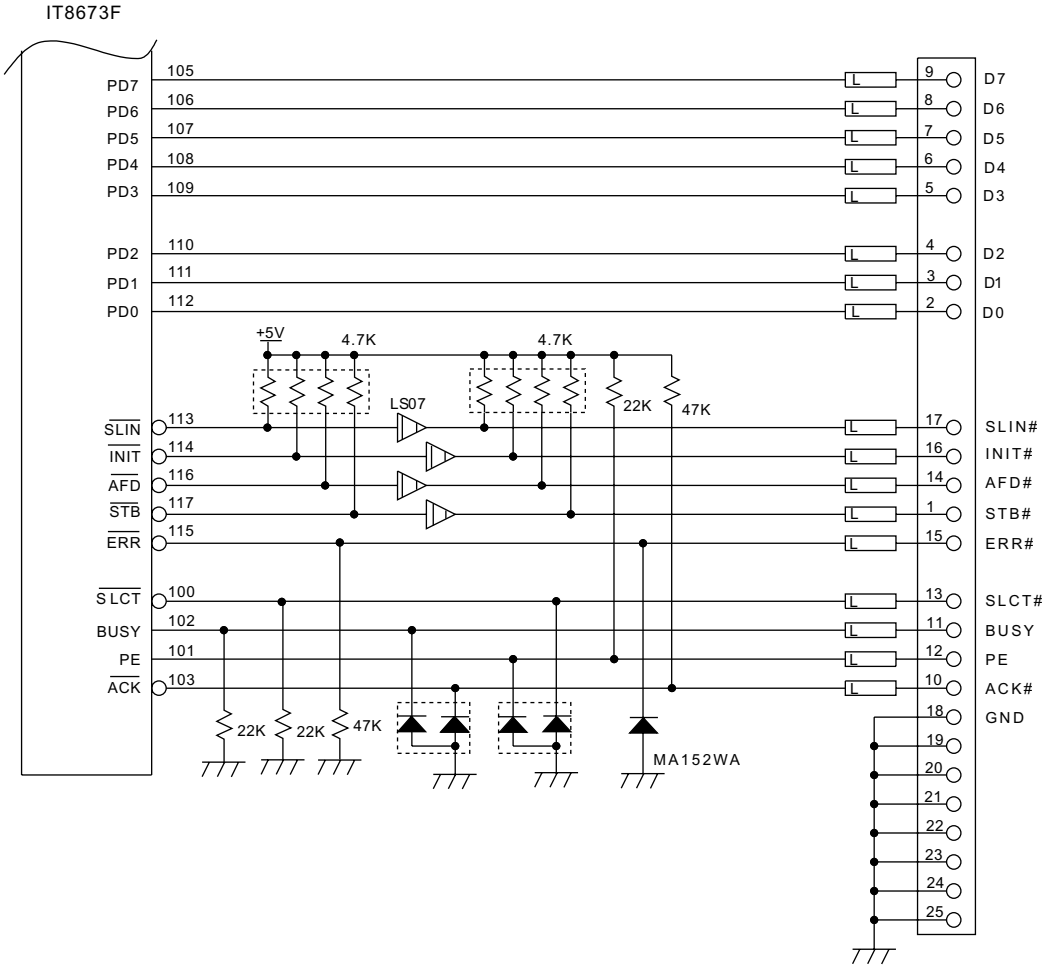
The I/O levels of the UART1,2 signals of the IT8673F1 are maintained at the TTL level. The ADM211 is used outside the UART2 for use as the driver or receiver of the RS-232-C interface. The ADM211 is an IC of 4 outputs and 5 inputs, and works only with a single power supply of +5V. Both COM1 and COM2 are used as the general-purpose serial ports toward the outside.

Baud rate	Register frequency division		Error rate (%)
	Hexadecimal	Decimal	
50	900H	2304D	0.160
75	600	1536	0.160
110	417	1047	0.186
150	300	768	0.160
300	180	384	0.160
600	C0	192	0.160
1200	60	96	0.160
1800	40	64	0.160
2000	3A	58	0.530
2400	30	48	0.160
3600	20	32	0.160
4800	18	24	0.160
7200	10	16	0.160
9600	C	12	0.160
19200	6	6	0.160
38400	3	3	0.060
56000	2	2	3.022

The Baud rate used is based on 1.8462MHz (13-frequency-divided from 24MHz).

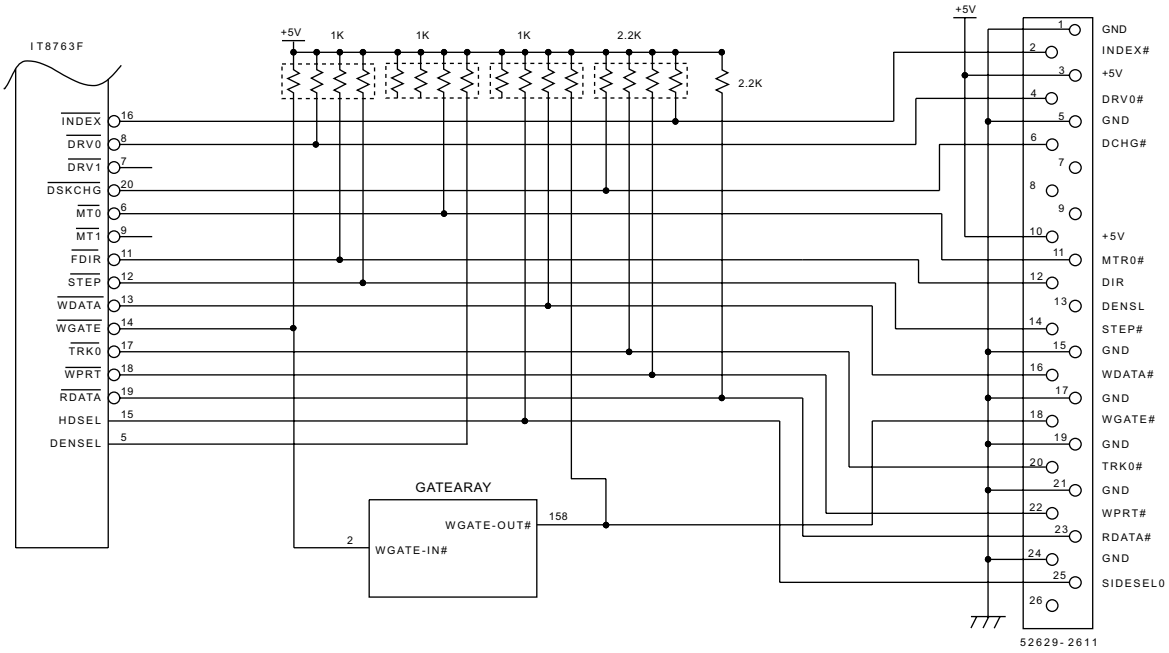
2.1.5.3 Parallel port interface circuit

The IT8673F is used as a parallel port control.
The parallel port of the IT8673F has a both-way function. When controlled by software, the data signals of the PD7-PD0 become both-way signals.
The output signals (SLIN, INIT, AFD, STB) for parallel port control are pulled up with 4.7kΩ of open drain output. However, since they are connected to the power supply terminal through diodes, Device 74LS07 is inserted at an external open collector buffer.
I/O address and interrupt of the parallel port are set up by the software.



2.1.5.4 FDD interface circuit

The IT8673F is used as a floppy disc controller.
The FDC functions of the IT8673F are compatible with Devices 765A, DP8473. The interface circuit is made AT-compatible.
All the output signals to the FDD are processed in the open collector mode, pulled up with 1kΩ.
All the input signals from the FDD are pulled up with 2.2kΩ.
Protection for the WGATE signal is assured by the hardware, using its own signal of FDDEN.



[Outline Operation of FDD]

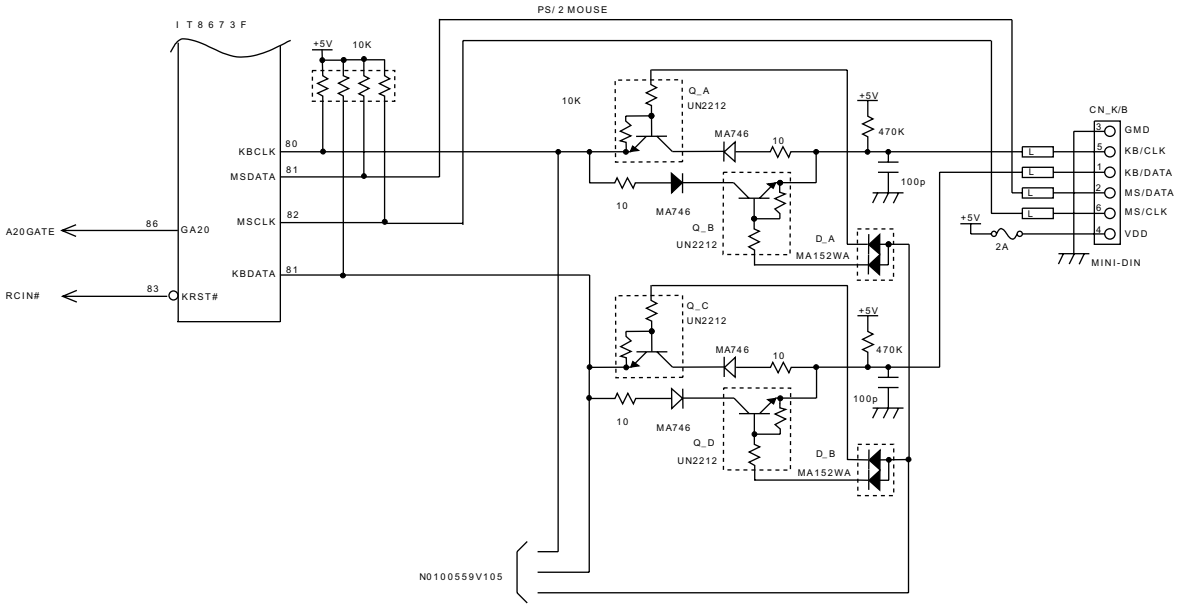
(1) As an outline operation, an FDD is selected to make the motor run, provided that the signals of both DRV0# and MTR0# are set at the low level.
(2) Each time the motor makes one revolution, an input of INDEX# signal is generated. This signal is used to identify that a diskette is present.
(3) The SIDESEL0 signal is set at the high level to select Head 0. The DIR signal is set at the high level to turn the head moving direction to the outer periphery.
(4) The STEP# signal (pulse) is output to move the head.
(5) The TRK0# signal is checked to confirm whether Track 0 has been detected. If detection fails, retrial from (4) is performed. If Track 0 cannot be detected after the specified number of retries, such a condition is regarded as an error.
(6) When Track 0 is detected, the RDATA# signal is used to read out the data from Track 0.
(7) In the write mode, the WRPRT# signal is checked. If it is at the low level, writing is disabled. Otherwise, writing is enabled.
(8) The SIDESEL#, DIR, and STEP# signals are specified to move the head to the required track.
(9) The WGATE# signal is made to stay at the low level to enable the FDD writing circuit.
(10) The write data are output from the WDATA# signal.
(11) Upon completion of writing, the WGATE# signal is made to stay at the high level.
(12) The replacement of a diskette is identified with the DCHNG# signal.

[FDD Interface Connectors]

Pin	Signal name	Pin	Signal name
1	GND	2	INDEX#
3	+5V	4	DRV0#
5	GND	6	DCHG#
7	NC	8	NC
9	DRATE0#	10	+5V
11	MTR0#	12	DIR
13	DENSEL	14	STEP#
15	GND	16	WDATA#
17	GND	18	WGATE#
19	GND	20	TRK0#
21	GND	22	WRPRT#
23	RDATA#	24	GND
25	SIDESEL0	26	NC

2.1.5.5 Keyboard controller circuit

The IT8673F is used for keyboard control.
The internal memory block of the IT8673F has programs for the keyboard control and the control with the main CPU.
The IT8673F internally converts the serial data sent from the keyboard into parallel data, and performs interrupt operation to inform the CPU of the entry of a key input.
The operation clock is set at 8MHz in the internal register.
The fuse connected to Pin 4 of the connector is used to protect the curl cord from burning in case the power supply circuit is short-circuited on the keyboard side.

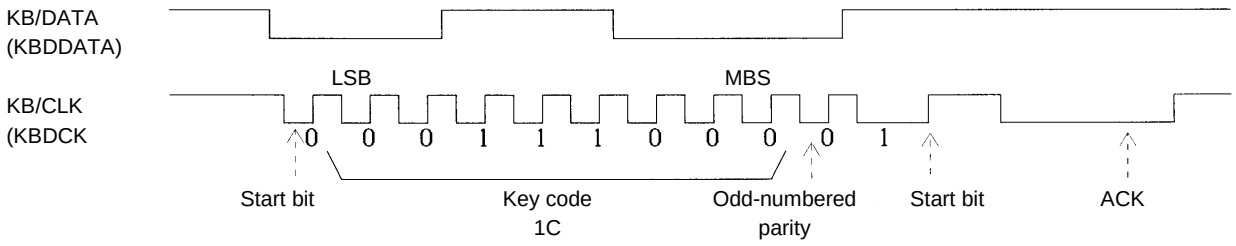


The transistor circuit is intended to control signals of the keyboard and the magnetic card controller. Control is actually undertaken by the magnetic card controller.
When the anodes of the diodes D_A and D_B are maintained at the high level, the transistors of Q_A~Q_D104 are turned ON and the keyboard signals are led to the keyboard controller.
When the anodes are turned low, the transistors are turned OFF to separate the keyboard controller from the keyboard. The keyboard is then connected to the magnetic card controller.
In the state of operation ready, both of the KBDDATA and KBDCK signals are maintained at the high level.
Regarding the serial data from the keyboard, one data lot is composed of 11 bits as shown below.

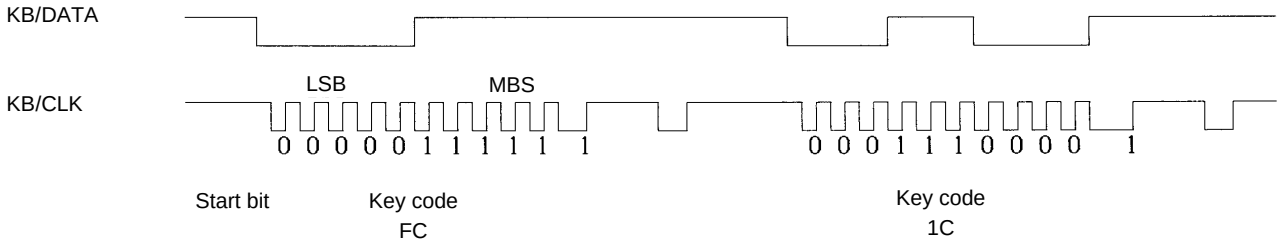
(1) Start bit ..... 1 bit (fixed at low level)
(2) Key code ..... 8 bits (LSB → MSB)
(3) Odd-numbered parity bit ..... 1 bit
(4) Stop bit ..... 1 bit (fixed at high level)

When the keyboard controller receives data from the keyboard, the clock line is once turned low as an ACK signal to the keyboard

When Key "a" is pressed (Make ..... Scan code "1C")

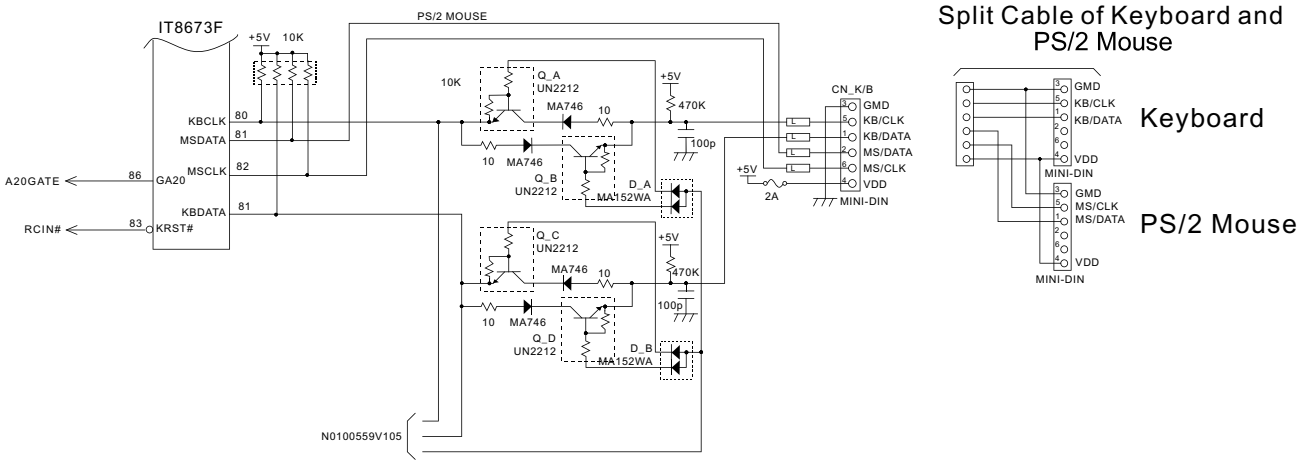


When Key "a" is released (Break ..... Scan code "F01C")



2.1.5.6 PS/2 mouse controller circuit

The IT8673F is used for PS/2 mouse control.
This IT8673F also functions as a keyboard controller, and is accordingly used in common with the PS/2 mouse.
The IT8673F internally converts the serial data sent from the PS/2 mouse into parallel data, and performs interrupt operation to inform the CPU of the entry of a mouse input.
Since the connector is used in common with the keyboard, it is necessary to use a converter connector when a PS/2 mouse is connected.

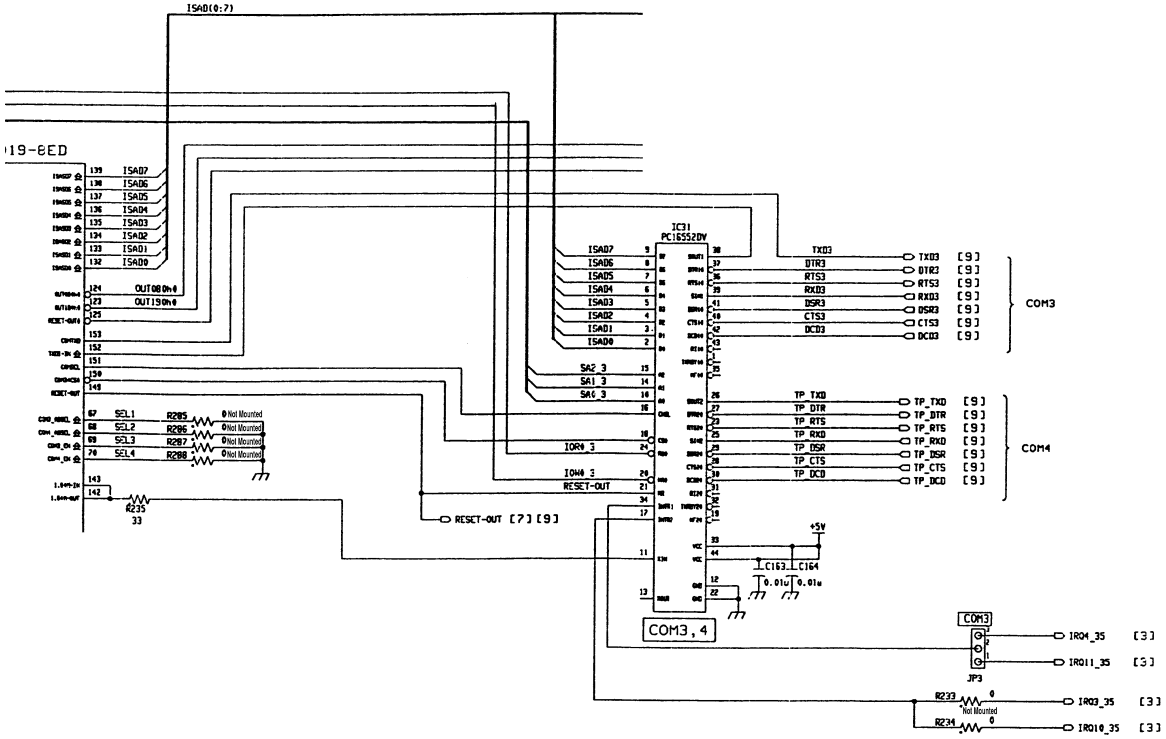


2.1.6 Serial port (COM3, 4)

The two 16C550 compatible serial port controllers (COMA and COMB) are incorporated in the PC16552D, independently of each other.
With the 1.84MHz clock (fixed) supplied from the outside, a Baud rate clock is generated. This port operates in an asynchronous mode.
The I/O addresses of these two controllers are decoded inside the gate array.

PC16552D	System	I/O address	Interrupt level
CAMA	COM3	3220~3227h	IRQ11 or IRQ3
COMB	COM4	3228~322Fh	IRQ10

The transmission data signal (TXD3) of the COM3 is used through customer and display changeover. The COM4 is used as an interface of the touch panel at the TTL level.



The COM3 and COM4 signal I/O of the PC16552D is processed at the TTL level. Therefore, the ADM211 is externally used for the driver and the receiver of the RS-2332-C interface.
The ADM211 is an IC of 4 outputs and 5 inputs, and works only with a single power supply of +5V.

Baud rate	Register frequency division		Error rate (%)
	Hexadecimal	Decimal	
50	900H	2304D	0
75	600	1536	0
110	417	1047	0.026
150	300	768	0
300	180	384	0
600	C0	192	0
1200	60	96	0
1800	40	64	0
2000	3A	58	0.690
2400	30	48	0
3600	20	32	0
4800	18	24	0
7200	10	16	0
9600	C	12	0
19200	6	6	0
38400	3	3	0
56000	2	2	2.860

The Baud rate used is when a 1.8432MHz oscillator is used.

2.1.7 VGA circuit (Refer to the page 4-4.)

The SM710 is used as a display controller for this system.
The SM710 is a controller designed in accordance with the SVGA (Super-VGA) Specification that enables color LCD display and CRT display of 640 × 480 and 800 × 600 dots.
The color TFT is an interface of 18 bits (6 bits × 3), while the color DSTN is an interface of 16 bits (8 bits × 2). The image thickness is controlled by the volume control.
A memory for Video with a capacity of 4Mbytes is incorporated. The interface toward the CPU is connected according to the PCI bus specification. The signal level is maintained at the TTL level. The basic clock for V-RAM access and display is produced by the internal PLL of the LSI, based on the 14.318MHz (14MHz) clock.
The SM710 executes initialize setting of the hardware by using the data bus (VMD0~22) of the Video-RAM when the reset condition is canceled.
There are the operational functions that can be set again by software and those available only by hardware setting.

Signal	1	0	Description
MD 0	7 MCLK	**8 MCLK**	External Memory Refresh to Command Delay
MD 1	3 MCLK	**4 MCLK**	External Memory RAS to CAS Delay(SGRAM)
MD 2	Reserve	**Reserve**	Reserve
MD 3	3 MCLK	**4 MCLK**	External Memory Pre-charge Time (SGRAM)
MD 4	MD 5 / MD 4		External Memory Column Address Control
MD 5	**1 / 0**	**8-bit column address**	
	1 / 1	9-bit column address	
	0 / X	10-bit column address	
MD 6	Reserve	**Reserve**	Reserve
MD 7	**Reserve**	Reserve	Reserve
MD 8	Color STN	**Color TFT**	Color LCD Type
MD 9	Inverted	**Normal**	TFT FPCLK Select
MD 10	MD 11 / MD 10		LCD Display Size
MD 11	1 / 1	1280 x 1024	
	1 / 0	1024 x 768	
	0 / 1	**800 x 600**	
	0 / 0	**640 x 480**	
MD 12	MD 14 / MD 13 / MD 12		Color TFT Interface Type
MD 13	0 / 0 / 0	9-bit .3bit/R.G.B.	
MD 14	0 / 0 / 1	12-bit 4bit/R.G.B.	
	0 / 1 / 0	**18-bit 6bit/R.G.B.**	
	0 / 1 / 1	24-bit 8bit/R.G.B.	
	1 / 0 / 0	24-bit 12+12bit	
	1 / 0 / 1	Analog	
	1 / 1 / 0	36-bit 18+18bit	
	1 / 1 / 1	Reserve	
MD 15	24-bit interface	**16-bit interface**	DSTN Interface Type
MD 16	Reserve (GPR70.0)	**Reserve**	User configration Bits
MD 17	Reserve (GPR70.1)	**Reserve**	User configration Bits
MD 18	Reserve (GPR70.2)	**Reserve**	User configration Bits
MD 19	Reserve (GPR70.3)	**Reserve**	User configration Bits

2.1.7.1 SM710 Pin Assignment

Pin No.	Signal name	IN/OUT	Functions
H 20	AD31		PCI System address data bus.
H 19	AD30	IN/OUT	
H 18	AD29		
G 20	AD28		
G 19	AD27		
G 18	AD26		
F 20	AD25		
F 19	AD24		
E 19	AD23		
E 18	AD22		
D 20	AD21		
D 19	AD20		
D 18	AD19		
C 20	AD18		
C 19	AD17		
C 07	AD16		
C 16	AD15		
A 17	AD14		
B 16	AD13		
A 16	AD12		
C 15	AD11		
B 15	AD10		
A 15	AD9		
C 14	AD8		
A 14	AD7		
C 13	AD6		
B 13	AD5		
A 13	AD4		
C 09	AD3		
D 11	AD2		
B 12	AD1		
A 12	AD0		
B 14	C/BE0#	IN/OUT	PCI Command/ byte enable signal. Active : Low
B 17	C/BE1#		
A 20	C/BE2#		
F 18	C/BE3#		
A 18	PAR	IN/OUT	PCI Bus parity signal
A 19	FRAME#	IN/OUT	PCI The signal used to indicate that the bus cycle is currently executed. Active : Low
B 18	TRDY#	IN/OUT	PCI The signal used to indicate the status that the target can perform data transfer.
C 18	IRDY#	IN/OUT	PCI The signal used to indicate the status that the initiator can perform data transfer.
B 19	STOP#	IN/OUT	PCI Request signal from the target to the initiator for the suspension of execution. Active : Low
C 17	DEVSEL#	IN/OUT	PCI Device select signal. Active : Low
E 20	IDSEL	IN	PCI The signal used to specify the target device.
J 20	PCICLK	IN	PCI System clock 33MHz/30MHz
K 18	RST#	IN	PCI Asynchronous reset signal. Active : Low
J 18	REQ	OUT	PCI Bus request signal. Active : Low
J 19	GNT#	IN	PCI Acknowledge signal to the REQ signal.
K 19	INTA#	OUT	PCI Interrupt signal. Connected with PCIINTD#.
Y 16	CKIN	IN	VGA clock input. Fixed at 14.3181MHz
K 20	REFCLK	IN	Clock for suspend refresh. 32.768MHz
L 17	MCKIN/LVDSCK	IN/OUT	Used as LVDSCK.
L 20	EXCKEN#	IN	Clock select signal. Low → CKIN, High → MCKIN

Pin No.	Signal name	IN/OUT	Functions	
J 04 H 01 H 03 G 02 G 03 F 01 H 04 G 01 H 02 J 03	MA0 MA1 MA2 MA3 MA4 MA5 MA6 MA7 MA8 MA9	OUT	Video-RAM Memory address.	
E 02	BA	OUT	Video-RAM Bank address.	
E 01	WE#	OUT	Video-RAM Write enable signal.	
F 02	CAS#	OUT	Video-RAM Column address strobe signal.	Active : Low
F 03	RAS#	OUT	Video-RAM Row address strobe signal.	Active : Low
D 01 K 01	CS0#/RAS0# CS1#/RAS1#	OUT	Video-RAM Chip select signal for SGRAM.	Active : Low
K 03	DSF/OE#	OUT	Video-RAM Block write signal for SGRAM.	Active : Low
E 03 D 02 C 06 B 06 Y 04 V 05 T 02 R 04	DQM0#/CAS0# DQM1#/CAS1# DQM2#/CAS2# DQM3#/CAS3# DQM4#/CAS4# DQM5#/CAS5# DQM6#/CAS6# DQM7#/CAS7#	OUT	Video-RAM Data mask signal for SGRAM.	Active : Low
J 02	SDCK	IN/OUT	Video-RAM Clock for SGRAM.	
J 01	SDCKEN	IN/OUT	Video-RAM Clock enable for SGRAM.	Active : High
T 01 R 02 P 03 P 01 N 02 M 03 M 01 L 02 L 01 L 03 M 02 N 01 N 03 P 02 R 01 R 03 W 04 W 02 W 03 Y 02 U 04 V 02 U 03 U 01	MD63 MD62 MD61 MD60 MD59 MD58 MD57 MD56 MD55 MD54 MD53 MD52 MD51 MD50 MD49 MD48 MD47 MD46 MD45 MD44 MD43 MD42 MD41 MD40	IN/OUT	Video-RAM Data bus.	

Pin No.	Signal name	IN/OUT	Functions
T 03	MD39		
U 02	MD38		Video-RAM Data bus.
V 01	MD37		
W 01	MD36		
Y 01	MD35		
V 03	MD34		
V 04	MD33		
Y 03	MD32		
A 06	MD31		
B 07	MD30		
C 08	MD29		
A 08	MD28		
B 09	MD27		
C 10	MD26		
A 10	MD25		
B 11	MD24		
C 11	MD23		
A 11	MD22		
B 10	MD21		
A 09	MD20		
C 09	MD19		
B 08	MD18		
A 07	MD17		
C 07	MD16		
C 01	MD15		
D 03	MD14		
C 03	MD13		
A 01	MD12		
B 03	MD11		
C 04	MD10		
B 04	MD9	IN/OUT	
B 05	MD8		
A 05	MD7		
C 05	MD6		
A 04	MD5		
A 03	MD4		
A 02	MD3		
B 01	MD2		
C 02	MD1		
B 02	MD0		
W 15	CRTHSYNC	OUT	CRT Horizontal sync signal output.
Y 15	CRTVSYNC	OUT	CRT Vertical sync signal output.
V 17	BLUE	OUT	CRT DAC output analog blue signal.
Y 18	GREEN	OUT	CRT DAC output analog green signal.
W 18	RED	OUT	CRT DAC output analog red signal.
L 19	ACTIVITY	IN/OUT	The status signal to indicate that the memory and I/O address are valid.
K 02	ROMEN#	OUT	VGA_BIOS ROM select signal. Active : Low
L 18	PDOWN#	IN	Power down enable signal. Active : Low
V 19	TEST0	IN/OUT	Test pin.
U 18	TEST1		

Pin No.	Signal name	IN/OUT	Functions
V 07	FDATA23	OUT	LCD Panel data.
U 07	FDATA22		
W 07	FDATA21		
Y 07	FDATA20		
V 08	FDATA19		
W 08	FDATA18		
Y 08	FDATA17		
V 09	FDATA16		
W 09	FDATA15		
Y 09	FDATA14		
V 10	FDATA13		
W 10	FDATA12		
Y 10	FDATA11		
Y 11	FDATA10		
W 11	FDATA9		
V 11	FDATA8		
Y 12	FDATA7		
W 12	FDATA6		
V 12	FDATA5		
Y 13	FDATA4		
W 13	FDATA3		
V 13	FDATA2		
Y 14	FDATA1		
W 14	FDATA0		
W 06	M/DE	OUT	LCD Data validity timing output for TFT color panel. Active : Low
Y 05	FP/FVSYNC	OUT	LCD Vertical signal.
V 06	FPSCLK	OUT	LCD Shift clock signal.
W 05	LP/FHSYNC	OUT	LCD Horizontal data latch signal.
Y 06	FPEN	OUT	LCD Panel enable signal.
U 14	FPVDDEN	OUT	LCD Power control signal. Active : High
V 14	VBIASEN	OUT	LCD Bias power supply (Vee) control signal. Active : High
N 20	PCLK	IN/OUT	Video-Port Pixel clock.
M 18	VREF	IN/OUT	Video-Port VSYNC or video decoder.
M 19	HREF	IN/OUT	Video-Port HREF or video decoder.
M 20	BLANK/TVCLK	IN/OUT	Video-Port blank output.
W 19	P15	IN/OUT	Video-Port RGB digital data.
V 20	P14		
U 19	P13		
T 18	P12		
U 20	P11		
T 19	P10		
T 20	P9		
R 18	P8		
R 19	P7		
R 20	P6		
P 18	P5		
N 17	P4		
P 19	P3		
P 20	P2		
N 18	P1		
N 19	P0		
W 17	IREF	IN	Current reference input for CRT.
Y 20	USR3	IN/OUT	General-purpose port.
W 20	USR2		
V 18	USR1/SDA	IN/OUT	Used as an SDA signal with CRT.
U 17	USR0/SCL	IN/OUT	Used as an SCL signal with CRT.

2.1.7.2 LCD interface circuit (Refer to the page 4-4.)

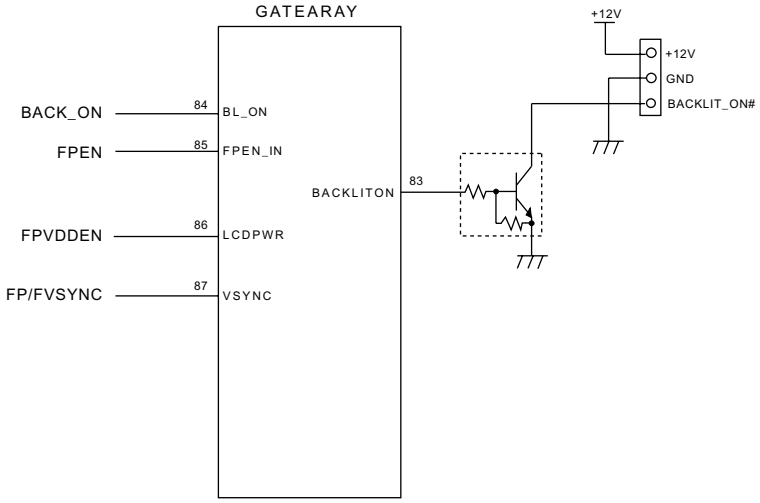
In regard to the interface signals for the LCD, various signals on the main PWB are used in common and the loopback PWB is used in order to enable connections with any type of the LCD. In this manner, LCD connections are modified.
The DSTN type color LCD calls for a volume control for brightness adjustment. Since the screen is divided, the upper screen data (UD-7) and the lower screen data (LD-7) are output at the same time.
The TFT type color LCD has a single screen. Therefore, the display data are output for R, G, and B, respectively.
In the SM710, the meaning of the output data changes according to the LCD panel mode.

Pin name	18bit TFT	16bit DSTN
FDATA23	Not used	Not used
FDATA22	Not used	Not used
FDATA21	R5	Not used
FDATA20	R4	Not used
FDATA19	R3	UD7
FDATA18	R2	UD6
FDATA17	R1	UD5
FDATA16	R0	UD4
FDATA15 (Note 1)	Not used	UD3
FDATA14 (Note 1)	Not used	UD2
FDATA13	G5	UD1
FDATA12	G4	UD0
FDATA11 (Note 1)	G3	Not used
FDATA10 (Note 1)	G2	Not used
FDATA9 (Note 1)	G1	Not used
FDATA8 (Note 1)	G0	Not used
FDATA7 (Note 1)	Not used	LD7
FDATA6 (Note 1)	Not used	LD6
FDATA5	B5	LD5
FDATA4	B4	LD4
FDATA3	B3	LD3
FDATA2	B2	LD2
FDATA1	B1	LD1
FDATA0	B0	LD0

(Note 1) According to the type of the LCD panel being connected, the resistor mounted on the PWB shall be changed.

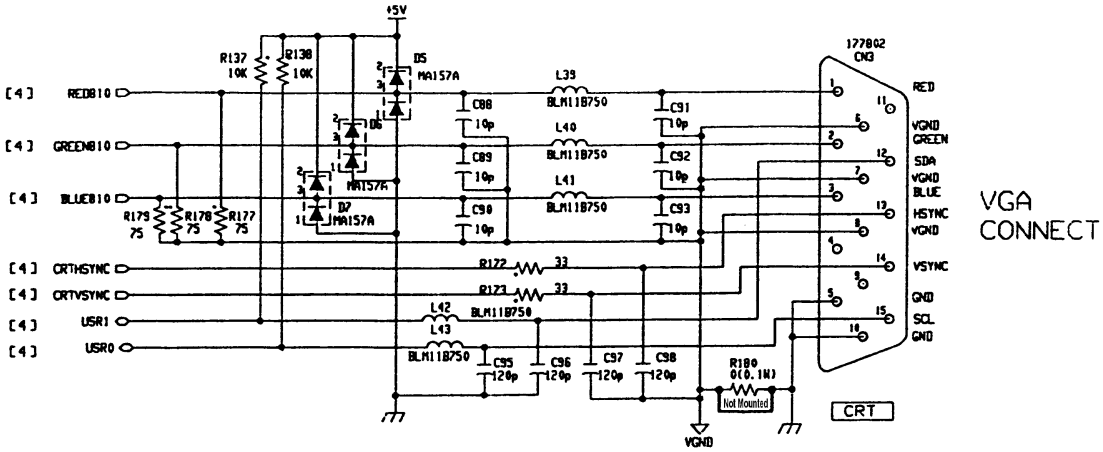
2.1.7.3 Back-Lite control circuit

A cold-cathode tube is used for the back light of the LCD.
The +12V power supply for driving is fed from an external inverter.
Assuming that the LCD is in the display mode (the FPEN signal at the high level), ON/OFF control of the power supply is effected by software.
This system performs controls in two positions; GPO_0 (Default = High) that is a general-purpose port of the FW82371EB and Bit0 (BACKEN) that is the I/O address 320H.
The Back-Lite is turned ON when the conditions of both are satisfied.
Generally, the control of FW82371EB is not used. Instead, ON/OFF control is performed by managing the BACKEN signal that is used for the control of the I/O address 320H.
The control hardware is located inside the gate array.



2.1.7.4 CRT interface

For a standard feature, this system is provided with an interface circuit for the CRT.
Simultaneous display is possible at the LCD and the CRT.

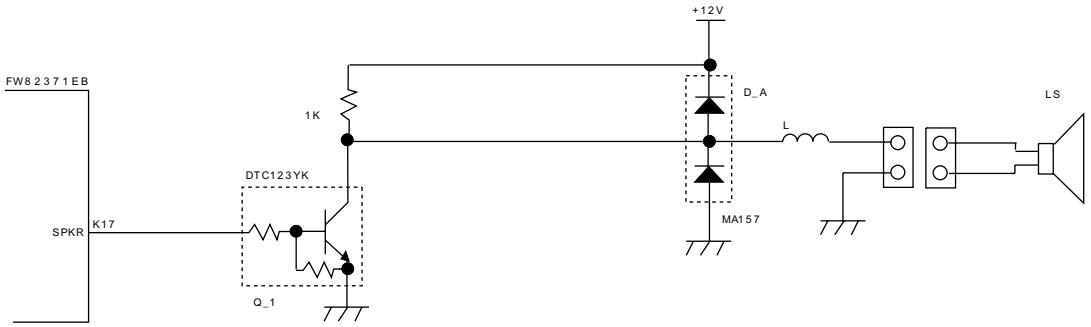


D-Sub Half 15-pin (Female)

Pin No	Signal name	Pin No	Signal name
1	RED	9	
2	GREEN	10	DGND
3	BLUE	11	
4		12	SDA
5	DGND	13	HSYNC
6	AGND	14	VSYNC
7	AGND	15	SCL
8	AGND	—	—

2.1.8 Piezoelectric buzzer circuit

For use as a signal for the piezoelectric buzzer, a rectangular wave output is generated from Pin 17 of the FW82371EB.
The diode D_A is used for the prevention of counter electromotive force.
The driving voltage is +12V.

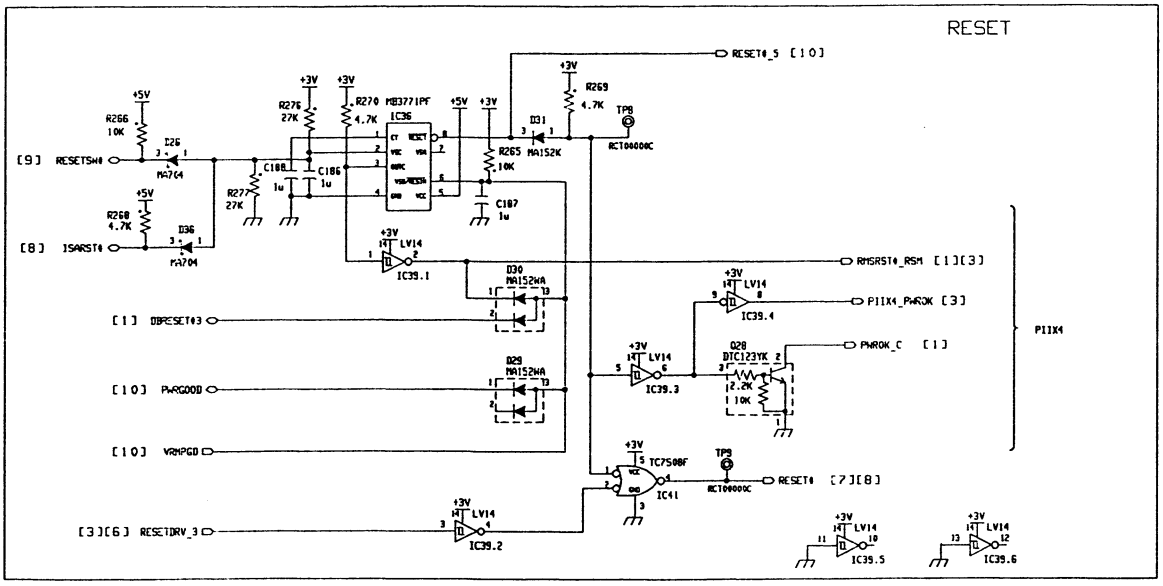


2.1.9 Hardware reset circuit

MB3771 is used in the hardware reset circuit.
When this MB3771 is used, a low level is maintained at Pin 8 of the RESET output terminal under the condition that the power supply voltage of VCC (Pin 5) is below the reference voltage (approx. 4.2V).
If the reference voltage is exceeded, the potential level at the RESET output terminal is turned high after the lapse of the predetermined time period (approx. 100msec), according to the capacitance connected to Pin 1.
In addition to power supply voltage level check, the MB3771 functions to receive the forced reset signal from the outside.
If the following conditions are satisfied as the external factors, the potential level at Pin 6 of the MB3771 will be lowered. Then, similarly as for the case when the power supply voltage is lowered, the potential level at Pin 8 of the RESET output terminal is turned low.

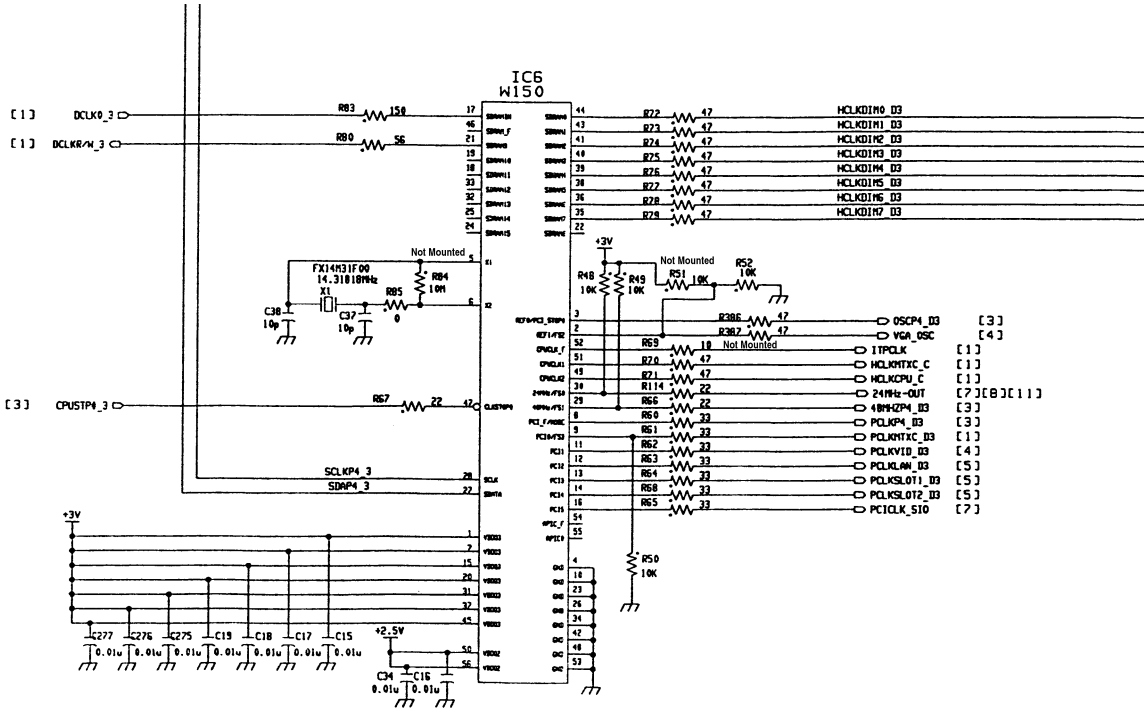
{External factors}

- The RESETSW# signal is turned to the low level. (RESET switch pressed)
- ISARST# is turned to the low level. (During execution by software)
- The PWRGOOD signal is turned to the low level. (POWER switch turned off)
- VRMPGD is turned to the low level. (Supervision of CPU voltage)
- DBRESET#3 signal is turned to the low level. (In case of debug)



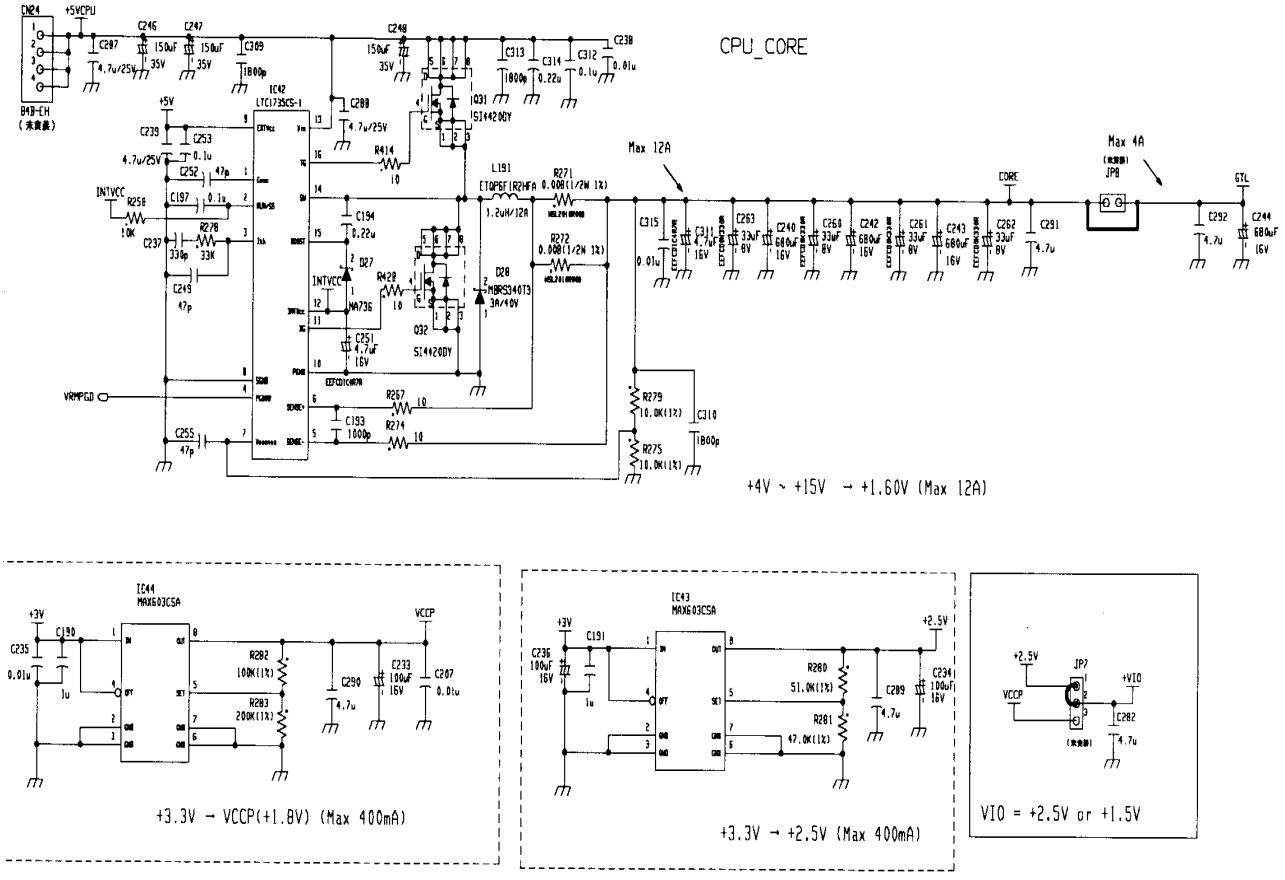
2.1.10 Clock

The basic clock for this system is fed from the clock generator (W150).
The basic clock of the W150 is maintained at 14.3181MHz and various clock signals are output for the CPU, chip set, PCI bus, SDRAM, USB, etc.



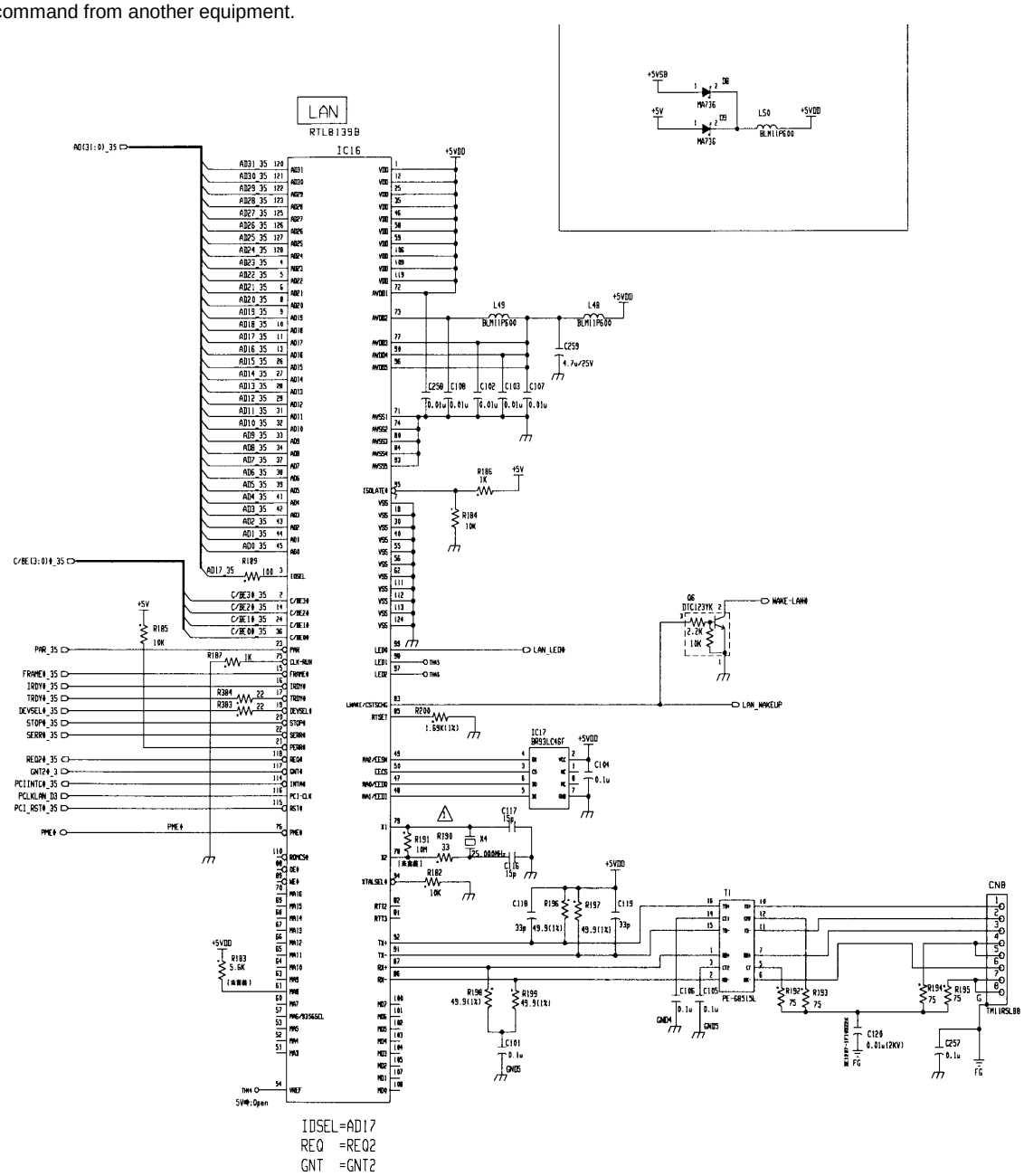
2.1.11 CPU_POWER

The LTC1735CS-1 is used as the core power supply circuit for the CPU.
The input power supply of +4V ~ +15V is fed from the power unit. This power unit generates a +1.6V core voltage that is to be supplied to the CPU.
The maximum current that can be supplied is 12A (coil and core rating).
Other voltages needed for and related to the CPU are +1.8V (VCCP) and +2.5V.



2.1.12 ETHERNET interface circuit

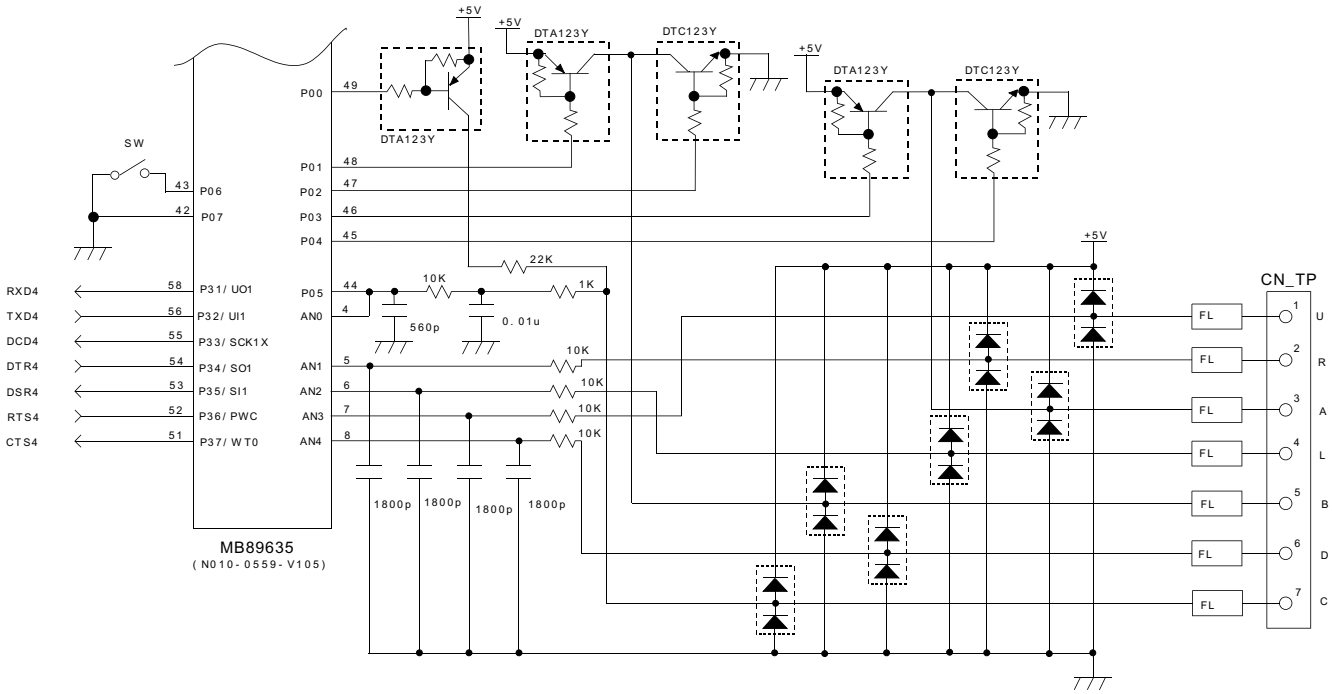
As one of the communication methods for this system, the ETHERNET is used as the communication line.
The ETHERNET circuit is composed of the control block on the main PWB and the transceiver block.
The RTL8139B(L) is used as a control LSI.
In the serial EEPROM (BR93LC46) connected to the outside, interface-related information and various information about the I/O addresses, interrupt, network's ID addresses, etc., are stored. At the time of starting, the RTL8139(L) is set up based on this EEPROM information.
The sync clock signal is generated from a 25MHz crystal oscillator connected.
During the reception of data, the serial data received from the transceiver are converted to parallel data, and various subsequent processes take place, such as comparison with the ID address, 32-bit CRC code check, 64-bit preamble removal, and the extraction of the data's main part. Since then, the data are transferred to the receiver buffer.
During data transmission, the transmitting data are once stored in the transmitter buffer and conversion is conducted from parallel data to serial data. Subsequently, the data are sent to the transceiver after the completion of the generation and addition of a 64-bit preamble code and a 32-bit CRC code. In case of the occurrence of collision, re-transmission is carried out.
In this system, it is possible to perform wake-up operation of the power supply through the ETHERNET.
Under the condition that the primary-side power supply is switched ON, it is possible to accomplish automatic power ON by the use of a command from another equipment.



2.1.13 Touch panel interface circuit

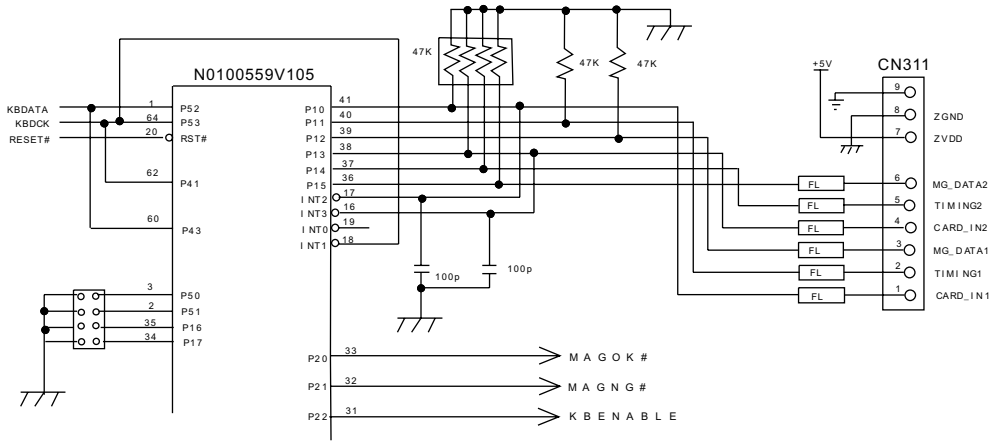
This system uses a touch panel of the resistance film type.
Control of the touch panel is effected by COM4 of the serial port.
Where the touch panel is pressed, the signal is analyzed by the one-chip CPU, N0100559V105, and sent to COM4.
The transfer Baud rate is 9600bps.
The operation mode is modified through switch setting.

For SW - ON (P06 terminal = Low) → Operation conforming to the Panasonic Specification (DOS)
For SW - OFF (P06 terminal = High) → Operation conforming to Windows



2.1.14 Magnetic card reader interface circuit

A magnetic card controller is accommodated in this system, in order to enable readout operation for the magnetic card according to the Second Track Specification (5 bits, 40 digits, recording density of 75BPI) of the ISO7810 Standard.
When the serial data input from the magnetic card are identified and correctly read out, all the data (start code, end code, check byte, etc.) read from the serial data are converted into the scan codes of the AT keyboard, and are transmitted to the keyboard controller.
At that time, the end part of the data is attached with “ENTER” as a scan code.
When data are sent to the keyboard controller, the CLKEN signal and the DATAEN signal are turned to the low level and the magnetic card controller is disabled in order not to send data to the outside keyboard.
Because of the requirements of the Standard, the card readout speed can cover 8 ~ 150cm/sec.
The CPU reads out scan codes from the keyboard controller, and again converts them into character codes.
For example, a magnetic card with 00012 written as the data may be read out. Then, since the start code (B), the end code (F), and the check byte (7) are already written in the card, the data come to coincide with the result of the ‘B00012F7 Return’ input from the keyboard in terms of operational sequence.
In case of failure in reading out the data from the card, the keyboard controller does not send out any scan code, but the error LED (red) is lit up.



[Magnetic card Second Track Specification]

Total No. of clocks..... Approx. 251 clocks (card as a whole)
Quantity of data ..... 5-bit × 40-digit = 200 bits (max.)
Bit configuration..... 5 bits (4 bits for data, 1 bit for odd parity)
Start code ..... B
End code ..... F
Separation code..... D
Timing signal ..... In the spaces from the start to first data bit (start code) and from the end data bit to the end, continuous binary codes “0” are recorded as the timing signal.

Scan Codes Applicable to the PC/AT Keyboard (For the Second Track)

Readout data	Output scan code					
	1	2	3	4	5	6
0	45	F0	45			
1	16	F0	16			
2	1E	F0	1E			
3	26	F0	26			
4	25	F0	25			
5	2E	F0	2E			
6	36	F0	36			
7	3D	F0	3D			
8	3E	F0	3E			
9	46	F0	46			
A	12	1C	F0	1C	F0	12
B (Start code)	12	32	F0	32	F0	12
C	12	21	F0	21	F0	12
D (Separation code)	12	23	F0	23	F0	12
E	12	24	F0	24	F0	12
F (End code)	12	2B	F0	2B	F0	12

ENTER	5A	F0	5A			

[Specification for Magnetic Card Control]

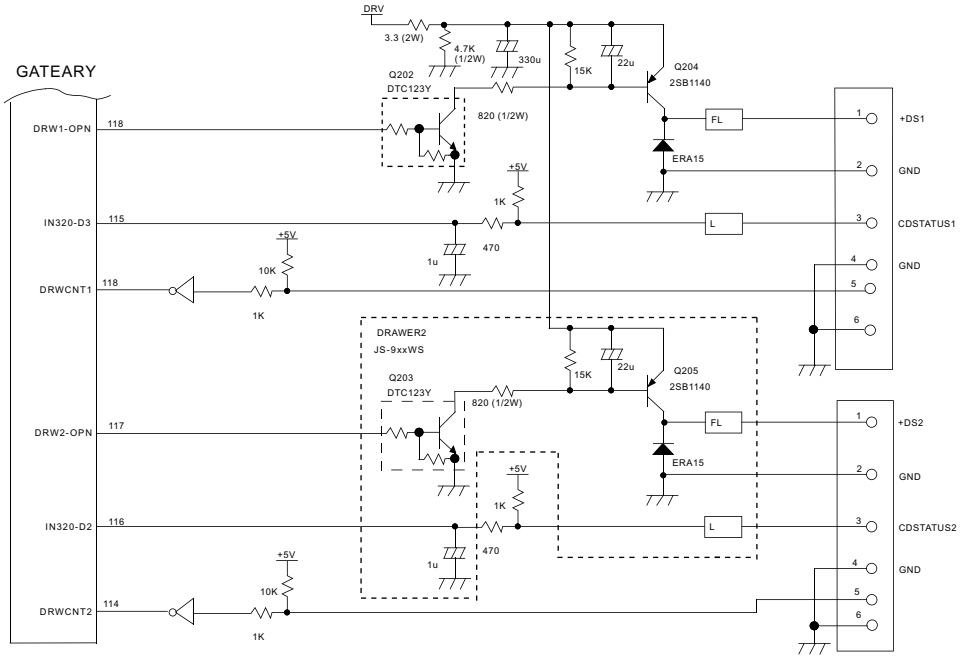
Contents of magnetic card control specified for the PENTIUM POS

(1) Connected to the keyboard connector.
(2) ISO 7810 compatible. (Second track)
(3) ID to be used is of the 5-bytes data with 0 included.
(4) For reference: ID = B00012F7
    a. “B” is the front byte. (Start code)
    b. “00012” is an ID of the 5-byte data with 0 included.
    c. “F” is the end byte. (End code)
    d. “7” is a check byte.

(5) Check byte calculation
    a) The header B is set in the binary data. (Result = 0bh)
    b) An exclusive OR is established with “0” of the front ID data. (Result = 0bh)
    c) An exclusive OR is established with “0” of the second ID data. (Result = 0bh)
    d) An exclusive OR is established with “0” of the third ID data. (Result = 0bh)
    e) An exclusive OR is established with “1” of the fourth ID data. (Result = 0ah)
    f) An exclusive OR is established with “2” of the fifth ID data. (Result = 08h)
    g) An exclusive OR is established with “F” of the end data. (Result = 07h)
    h) The above-mentioned result is compared with “7” for the check byte.

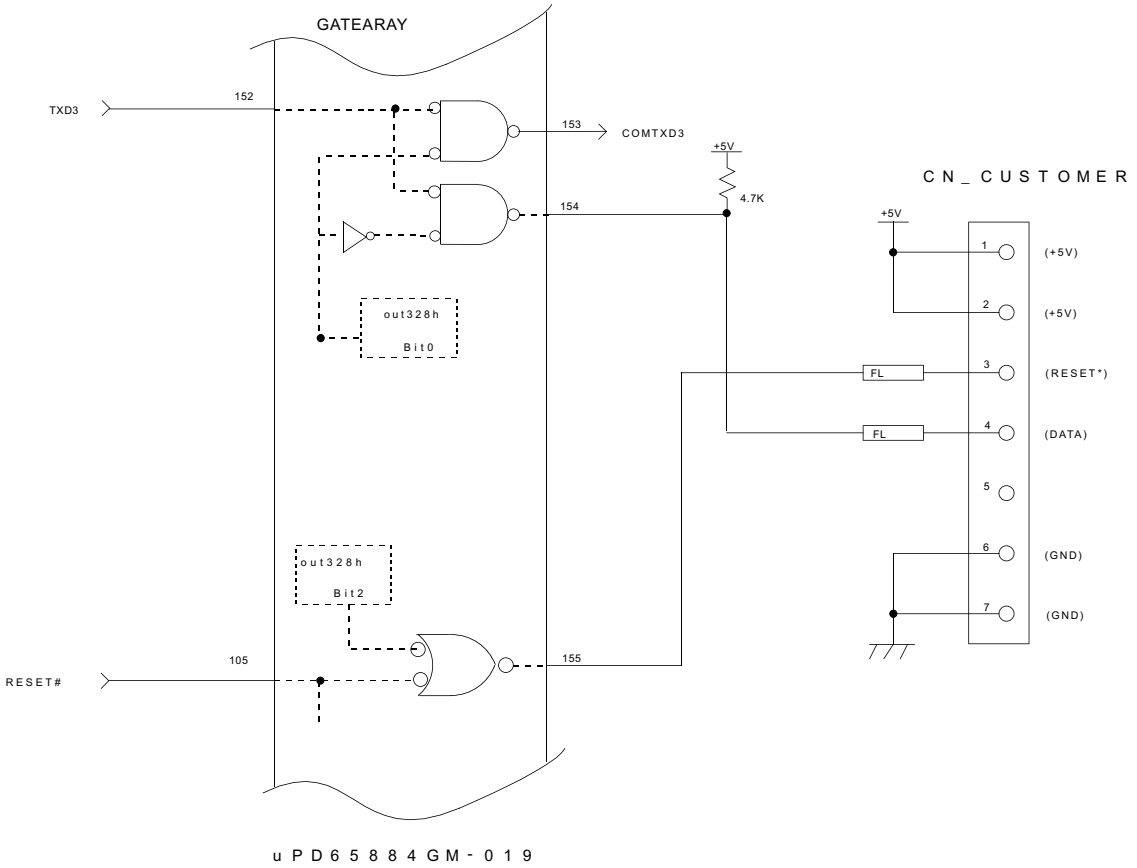
2.1.15 Cash-Drawer interface circuit

As an integrated POS, two Cash-Drawer interface circuits are provided.
To drive the cash drawer, 328H of the I/O port is used for interface control.
Drawer 1 is controlled with Bit 4 of Address 328, while Drawer 2 is controlled with Bit 5.
When “1” is written in Bit 4, a high level output is generated at the DRW1-OPN signal (Pin 118) of the GATEARRAY (µPD65884GM). Then, Transistor Q25 is turned ON via Q24 and approx. +15V is supplied as the +DS1 signal.
When “1” is written in Bit 5, a high level output is similarly generated at the DRW2-OPN signal (Pin 117) of the GATEARRAY. Then, Transistor Q26 is turned ON and approx. +15V is supplied as the +DS2 signal.
The drawer opening time can be selected by the use of Switches 3 and 4 of the DIPSW2.
The default setting is about 140msec.
Inside the GATEARRAY circuit, there is a circuit intended to avoid the simultaneous operation of Drawer 1 and Drawer 2.
CDSTATUS1 and CDSTATUS2 are the drawer status signals. For the type of a drawer to be connected, the logic may be reversed.
In the present circuit, a low level is defined as the status when a drawer is closed. When using a drawer for which the logic has been reversed, the section is short-circuited between Pin 5 and Pin 6 of the connector. (Arranged with a cable)
By making DRWCNT1 (Pin 119) and DRWCNT2 (Pin 114) of the GATEARRAY circuit turned to the high level, arrangements for exclusive OR (EXOR) are made for the signals of DRWST1 (Pin 115) and DRWST2 (Pin 116) and also for the GATEARRAY interior.
As a result, the software can conclude the judgment of Open or Close.
By reading out Address 32D of the I/O port, the logic can be defined at Bit 3 and 2.



2.1.16 Customer display interface

A fluorescent display light tube of 20 digits × 1 line or 2 lines is used as a customer display.
The driving voltage for the customer display is +5V, the transmission data need be the serial data at the TTL level.
The serial data are used through the changeover of the TXD signal (TTL) of COM3 by the aid of software.
Since the TXD signal of COM3 is used also as the interface signal (TXD3-OUT) for the RS-232-C, the above-mentioned customer display cannot be used while COM3 is used externally.
The reset signals for hardware resetting in case of Power ON and for software control are used as the reset signals for the customer display.



2.1.17 Power ON/OFF circuit

2.1.17.1 Power ON

The conditions to make power ON are categorized to the following three cases:
The conditions and conditional sequences are specified below.

(Condition 1.....ON with the primary-side switch. Condition.....JP9 is short-circuited.)
- The primary-side Power switch is turned ON.
- A power supply of +5VSB is supplied.
- The AC_ON_SB signal is turned to the high level.
- Potential at Pin 8 of HCT74 (IC48) is turned low.
- Since JP9 is short-circuited, the PS_ON# signal is turned to the low level.
- The secondary side output of the power supply is turned ON.

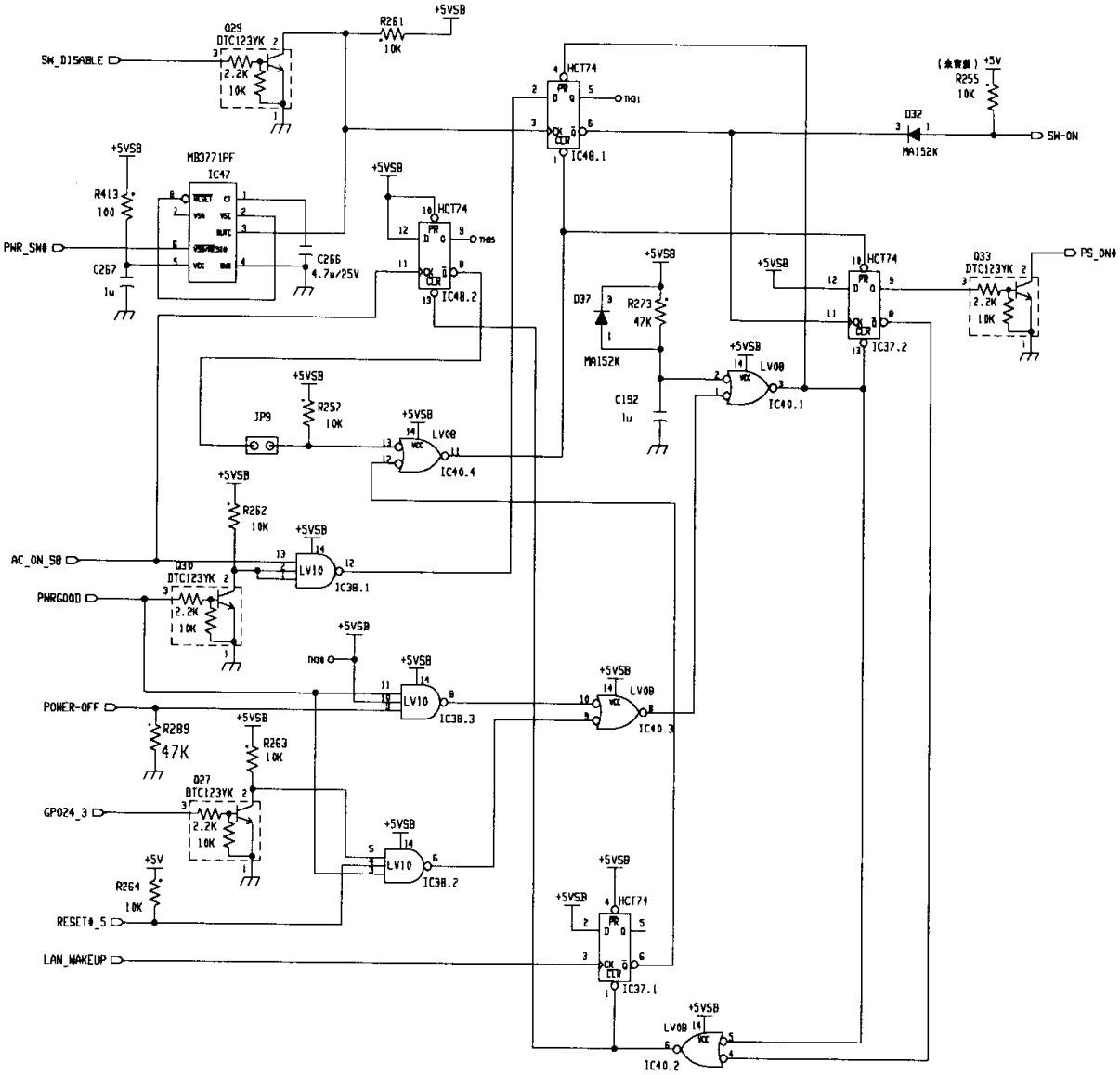
(Condition 2.....ON with the secondary-side power switch. Condition.....Standby state with the primary side turned ON.)
- The primary-side Power switch is turned ON and the standby state is assumed. (AC_ON_SB at high level)
- The secondary-side Power switch is turned ON and the PWR_SW# signal is turned low.
- Potential at Pin 3 of MB3771 (IC47) is turned high and the PS_ON# signal is turned low.
- The secondary side output of the power supply is turned ON.

(Condition 3.....ON through the LAN. Condition.....Standby state with the primary side turned ON.)
- The primary-side Power switch is turned ON and the standby state is assumed. (AC_ON_SB at high level)
- The command for Power ON is output through the LAN and the LAN_WAKEUP signal is turned high.
- Potential at Pin 6 of HTC74 (IC37) is turned low and the PS_ON# signal is turned low.
- The secondary side output of the power supply is turned ON.

2.1.17.2 Power OFF

The conditions to make power OFF are as follows:

- The secondary-side Power switch is pressed. (The standby state is assumed.)
- An OFF command output is generated by software. (The GPO24_3 signal is turned low.)
- An OFF command output is generated by hardware. (The POWER_OFF signal is turned low.)
  (In particular in this case, this condition arises when the power supply is turned off in any case other than the normal state, such as a service interruption, etc.)



2.1.17.3 Battery backup circuit

This system is provided with a battery backup function to be available in case of a service interruption, with a battery connected to the power unit.
The battery backup circuit is used for functional ON/OFF control with the aid of software.
The software checks the battery voltage (BATT_VOLT) and switches on the required function when the voltage is found to be above the specified level.
When the function is turned ON and the AC power supply is turned OFF (AC_ON signal turned low), the BATT_ON signal is turned high and +5V, +3.3V, and +5VCPU (about 8V) are supplied from the battery in the power unit.
Since the supply of +12V is effected, the Back-Lite of the LCD cannot be lit up.
The backup feature is canceled in the following 3 cases:

- When the function is switched OFF with software.
- When forced OFF is executed from hardware in 2 to 5 minutes (set by software) after the start of backup action.
- When the battery voltage lowers and the +5V voltage is found to be below the specified level (approx. 4.2V).

Battery charge is conducted inside the power unit while the AC power supply is ON.
The battery to be used is of the nickel-cadmium type of 7.2V (1.2V $\times$ 6 cells), 1500mA.
The control circuit is accommodated in the GATEARRAY.
For more details, refer to the instruction manual for the GATEARRAY and the internal equivalent circuit.

2.1.18 GATEARRAY (μPD65884GM-019-BED) (Refer to the page 4-8)

Functions of the GATEARRAY (μPD65884GM-019-BED) are described below.
For more details in regard to the internal circuits, refer to the instruction manual for the GATEARRAY separately furnished.

2.1.18.1 Internal functions

The major functions provided inside the GATEARRAY are as specified below.

- Address decoder for COM3 and COM4
- Address decoder for POST LED
- Control circuit for cash drawer
- Clock frequency divider circuit
- FDD gate signal control circuit
- Customer Display control circuit
- POS individual control circuit
- LCD timing control circuit
- Power supply control circuit

2.1.18.2 GATEARRAY Pin Assignment

Pin No.	Signal name	IN/OUT	Functions	Common
2	WGATE_INN	IN	FDD WE (Write Enable)# signal input pin. (Super I/O)	FDD
156	SA0	IN	Address bus conforming to the ISA Specifications.	Common
157	SA1			
3 | 16	SA2 | SA15			
17	BATEN_IN	IN	Battery backup enable input pin. Active : High	AC Detect
18	TMR_SET1	IN	Battery backup time setting 1.	Bvack-up Timer
19	TMR_SET0	IN	Battery backup time setting 2.	
22	O322_D7	OUT	Output port 0322h bit7 output pin. Connected to TMR_SET1.	I/O 0322h
23	O322_D6	OUT	Output port 0322h bit6 output pin. Connected to TMR_SET0.	
24	O322_D5	OUT	Output port 0322h bit5 output pin. (Not used)	
25	O322_D4	OUT	Output port 0322h bit4 output pin.	
26	O322_D3	OUT	Output port 0322h bit3 output pin.	
27	O322_D2	OUT	Output port 0322h bit2 output pin. (Not used)	
28	O322_D2N	OUT	Reversed output pin of output port 0322h bit2.	
29	O322_D0	OUT	Output port 0322h bit0 output pin.	
30	IN32D_D4	IN	Battery connection identification input pin. High: Not connected, Low: Connected.	I/O 032Dh
31	IN321_D7	IN	Battery level input pin.	IN 0321h
32	IN321_D6	IN	Battery level input pin.	
33	IN321_D5	IN	Battery level input pin.	
34	POWR_OFF	OUT	Secondary side power OFF control output. Active : High	Back-Reset
35	SW_ON_IN	IN	Secondary side power control signal input pin. Active : High	AC Detect
36	FLAGCLRN	IN	AC power OFF detect. Flag clear input. Active : Low	
37	BATT_ON	OUT	Battery backup ON output. Active : High	
38	PWRINTN	OUT	Power OFF interrupt output. Active : Low	
39	AC_ON-IN	IN	AC power detect input pin. Active : High	
43	PORTEN	IN	Hard enabled pin for POS exclusive port (0320h ~ 032Fh). Active : Low	PORT CNT
44	IN32D_D5	IN	Input port 032Dh bit5 input pin.	IN 032Dh

Pin No.	Signal name	IN/OUT	Functions	Common
45	DRAW_ST0	IN	Cash-Drawer open time setting Bit0.	DRAWER
46	DRAW_ST1	IN	Cash-Drawer open time setting Bit1.	
47	IN32D_D0	IN	Input Port 032Dh bit0 input pin.	
48	IN32D_D1	IN	Input Port 032Dh bit1 input pin.	IN 032Dh
49	IN32D_D6	IN	Input Port 032Dh bit6 input pin.	
50	IN32D_D7	IN	Input Port 032Dh bit7 input pin.	
51	IN324_D5	IN	Input Port 0324h bit5 input pin.	
52	IN324_D4	IN	Input Port 0324h bit4 input pin.	IN 032Dh
53	IN324_D3	IN	Input Port 0324h bit3 input pin.	
54	IN324_D2	IN	Input Port 0324h bit2 input pin.	
55	IN324_D1	IN	Input Port 0324h bit1 input pin.	
56	IN324_D0	IN	Input Port 0324h bit0 input pin.	
57	ITEST1	IN	Test pin. Not connected.	
58	SEL160N	IN	170FR/160FR changeover pin.	DECODE
59	24MHz_IN	IN	24.0MHz clock input pin.	CLOCK
61	EXISARDN	IN	ISA extension bus control signal from outside.	DATA-ISAEX
62	9MSEC_OT	OUT	CLOCK 9msec period output pin.	CLOCK
63	71MSC_OT	OUT	CLOCK 7msec period output pin.	
64	SFTRT_EN	IN	Software reset enable input pin.	Back-Reset
65	ITEST2	IN	Test pin. Not connected.	
66	IORSTN	OUT	Reset output pin. Active : Low	Back-Reset
67	CM3_ASEL	IN	COM3 address select. High:3220h~Low:03E8h~	
68	CM4_ASEL	IN	COM4 address select. High:3228h~, Low:02E8h~	COM ADDRESS
69	COM3_EN	IN	COM3 hardware control. High:COM3 Enable , Low:Disable	
70	COM4_EN	IN	COM4 hardware control. High:COM4 Enable , Low:Disable	
71	IN32C_D7	IN	71 : Input Port 032Ch bit7 input pin. (Not used)	
72	IN32C_D6	IN	72 : Input Port 032Ch bit6 input pin. (Not used)	IN 032Ch
73	IN32C_D5	IN	73 : Input Port 032Ch bit5 input pin. (Not used)	
74	IN32C_D4	IN	74 : Input Port 032Ch bit4 input pin. (Not used)	
75	IN32C_D3	IN	75 : Input Port 032Ch bit3 input pin. (Not used)	
76	IN32C_D2	IN	76 : Input Port 032Ch bit2 input pin. (Not used)	
77	IN32C_D1	IN	77 : Input Port 032Ch bit1 input pin. (Not used)	
78	IN32C_D0	IN	78 : Input Port 032Ch bit0 input pin. (Not used)	
82	ITEST3	IN	Test pin. Not connected.	
83	BACKLTON	OUT	LCD Back-Light control output signal. Active : High	
84	BL_ON	IN	LCD Back-Light control input pin. Active : High	LCD_CONT
85	FPEN_IN	IN	LCD enable input pin. Active : High	
86	LCDPWR	IN	LCD power control input pin. Active : High	
87	VSYNC	IN	Display Vsync input pin.	
88	LCD_1Q	OUT	LCD control timing 1. Active : High	
89	LCD_2QN	OUT	LCD control timing 2. Active : Low	
90	LCD_3Q	OUT	LCD control timing 3. Active : High	
91	COLORCRN	OUT	LCD control timing 4. Active : Low	
92 | 99	SD7 | SD0	IN/OUT	Data bus conforming to the ISA Specifications.	DATA-SD
102	IORN	IN	ISA I/F control signal. I/O Read signal. Active : Low	
103	IOWN	IN	ISA I/F control signal. I/O Write signal. Active : Low	
104	AEN	IN	ISA I/F control signal. Address Enable signal.	

Pin No.	Signal name	IN/OUT	Functions	Common
105	RESET_INN	IN	ISA I/F control signal. RESET input.	RESET
106	TMODE	IN	Test pin. Not connected.	
107	ITEST0	IN	Test pin. Not connected.	
108	OTEST0	OUT	Test pin. Not connected.	
109	O320_D3N	OUT	Reversed output pin of Output Port 0322h bit3. (Not used)	I/O 0320h
110	O320_D2N	OUT	Reversed output pin of Output Port 0322h bit2. (Not used)	
111	O320_D1N	OUT	Reversed output pin of Output Port 0322h bit1. (Not used)	
112	O320_D0N	OUT	Reversed output pin of Output Port 0322h bit0. (Not used)	
113	DRAWE_EN	IN	Cash Drawer Enable pin. Active : High	DRAWER
114	DRWCNT2	IN	Cash Drawer2 Type Detect pin.	IN 032Dh
115	IN32D_D3	IN	Drawer1 status input.	
116	IN32D_D2	IN	Drawer2 status input.	
117	DRW2_OPN	OUT	Cash Drawer2 Open output pin. Active : High	DRAWER
118	DRW1_OPN	OUT	Cash Drawer1 Open output pin. Active : High	DRAWER
119	DRWCNT1	IN	Cash Drawer1 Type Detect pin. McD-Type:High ,SECR-Type:Low	IN 032Dh
123	OT_190HN	OUT	Output Port 0190h output pin for POST_LED select. Active : Low	POST
124	OUT_80HN	OUT	Output Port 0080h output pin for POST_LED select. Active : Low	
125	REST_OTN	OUT	In-phase output of REST#-IN input signal. Active : Low	RESET
126	OT329_D7	OUT	Output Port 0329h bit7 output pin. (Not used)	I/O 0329h
127	OT329_D6	OUT	Output Port 0329h bit6 output pin. (Not used)	
128	OT329_D5	OUT	Output Port 0329h bit5 output pin. (Not used)	
129	OT329_D4	OUT	Output Port 0329h bit4 output pin. (Not used)	
130	OT329_D1	OUT	Output Port 0329h bit1 output pin. (Not used)	
131	OT329_D0	OUT	Output Port 0329h bit0 output pin. (Not used)	
132 | 139	ISAD0 | ISAD7	IN/OUT	Data bus for ISA I/F extension.	DATA-ISAEX
141	OT328_D1	OUT	Output Port 0328h bit1 output pin. (Not used)	I/O 0328h
142	1_84M_OT	OUT	1/13 of the 59-pin input clock output generated.	CLOCK
143	1_84M-IN	IN	1.84MHz clock input pin.	
144	OT328_D3	OUT	Output Port 0328h bit3 output pin. (Not used)	I/O 0328h
145	OT328_D4	OUT	Output Port 0328h bit4 output pin. (Not used)	
146	OT328_D5	OUT	Output Port 0328h bit5 output pin. (Not used)	
147	OT328_D6	OUT	Output Port 0328h bit6 output pin. (Not used)	
148	OT328_D7	OUT	Output Port 0328h bit7 output pin. (Not used)	
149	RESET_OT	OUT	Reversed output of REST#-IN input signal. Active : Low	RESET
150	COM34CSN	OUT	Chip Select signal for COM3 and COM4. Active : Low	COM ADDRESS
151	COMSEL	OUT	Changeover signal for COM3 and COM4. COM3:High , COM4:Low	COM ADDRESS
152	TXD3_IN	IN	UART COM3 TxD signal output pin.	CUSTOMER
153	COMTXD	OUT	COM3 TxD signal.	
154	CUSTTXD	OUT	CUSTOMER-LCD Data signal.	
155	CUST_RTN	OUT	CUSTOMER-LCD Reset signal. Active : Low	I/O 0328h
158	WGAT-OTN	OUT	FDD WE# control signal. Active : Low	FDD

2.1.19 Optional interface (Refer to the page 4-5 CN7)

As an optional connector, the system is provided with a connector intended to make connections of the PCI (Peripheral Component Interconnect) buses for two slots.
When a card conforming to the PCI Bus Specifications is mounted, it becomes possible to have a variety of functions externally. The PCI buses conform to the Board Specifications of +5V.

Pin	Signal name	Pin	Signal name	Pin	Signal name	Pin	Signal name
1	-12V	2	GND	3	+12V	4	+12V
5	GND	6	GND	7	+5V	8	+5V
9	INTA#	10	INTB#	11	INTC#	12	INTD#
13	Reserve	14	Reserve	15	Reserve	16	SERIRQ
17	Reserve	18	GND	19	RST#	20	CLK0
21	CLK1	22	GND	23	GNT0#	24	REQ0#
25	GNT1#	26	IREQ1#	27	PME#	28	+5V
29	+5V	30	AD31	31	AD30	32	AD29
33	+3.3V	34	AD28	35	AD27	36	AD26
37	AD25	38	AD24	39	C/BE3#	40	AD23
41	+3.3V	42	GND	43	AD22	44	AD21
45	AD20	46	AD19	47	GND	48	+3.3V
49	AD18	50	AD17	51	AD16	52	C/BE2#
53	+3.3V	54	GND	55	FRAME#	56	IRDY#
57	+3.3V	58	TRDY#	59	DEVSEL#	60	GND
61	GND	62	STOP#	63	LOCK#	64	+3.3V
65	+3.3V	66	GND	67	SERR#	68	PAR
69	C/BE1#	70	AD15	71	AD14	72	+3.3V
73	GND	74	AD13	75	AD12	76	AD11
77	AD10	78	GND	79	GND	80	AD9
81	AD8	82	C/BE0#	83	AD7	84	+3.3V
85	+3.3V	86	AD6	87	AD5	88	AD4
89	AD3	90	GND	91	GND	92	AD2
93	AD1	94	AD0	95	+5V	96	+5V
97	+5V	98	+5V	99	+5V	100	+5V

3 Test Program and Power Supply Check

3.1 Voltage checks on the MAIN PWB

1) Prior to inspection, all loads, such as the LCD unit, HDD, fluorescent display tube, peripheral PWBs, etc., shall be connected.

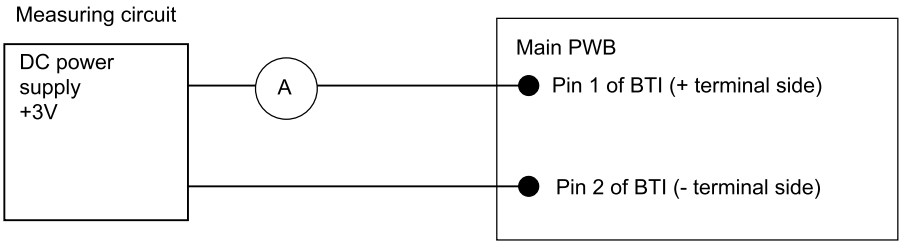
2) For the AC power supplies, each power input shall conform to the requirements of rating.

3) Voltage values

Item	Measuring point			Standard [V]	Remarks
+3V	CN26_8pin	-	TP6(GND	+3.3V±0.16	
+5V	CN26_18pin	-	TP6(GND)	+5.0V±0.25	
+5VSB	CN26_1pin	-	TP6(GND)	+5.0V±0.25	
+12V	CN26_4pin		TP6(GND)	+12.0±0.6	
-12V	CN26_28pin	-	TP6(GND)	-12.0±0.6	
+15V	CN26_2pin	-	TP6(GND)	+13.5~20	
CORE	JP8	-	TP5(GND)	+1.6±0.13	
VCCP	JP7_3pin	–	TP4(GND)	+1.8±0.09	
+2.5V	JP8_2pin	–	TP4(GND)	+2.5±0.12	
RTCVCC	TR1(RTCVCC)	-	TP4(GND)	+3.0, +0.4, -0.6	Lithium battery (with the power turned off)

4) Measurement of currents in the RTC backup circuit

Standard value	2~15μA



- The battery shall be disconnected during measurement.
- Measurement shall be performed with the power supply turned off.

Note) Standard values shall be obtained through measurements at a room temperature.

3.2 Oscillation frequency check

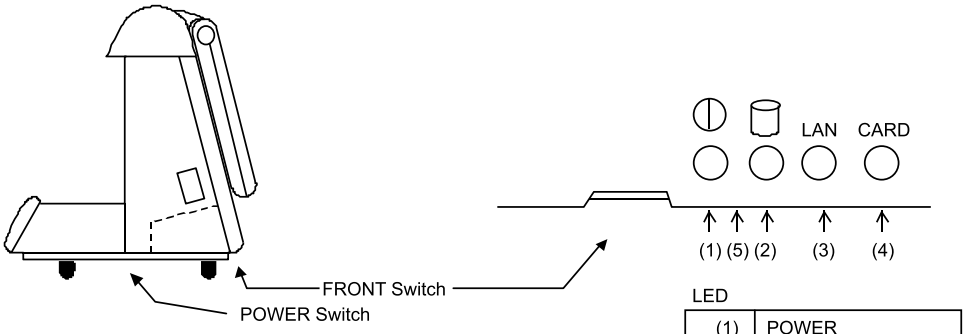
1) Clock oscillation frequency

Item	Measuring point	Standard	Remarks
X1	R85 — TP6(GND)	14.318Mhz±0.03%	
X2	R123 — TP6(GND)	32.768Mhz±0.005%	
X4	C116 — TP6(GND)	25.000Mhz±0.03%	
X5	C134 — TP4(GND)	10.000Mhz±2%	

2) Clock generator output frequency

Item	Measuring point	Standard	Remarks
HCLKCPU	R71 — TP6(GND)	64.516Mhz~66.9MHz	
HCLKDIM	R76 — TP6(GND)	64.516Mhz~66.9MHz	
PCLKSLOT2	R68 — TP6(GND)	30.03Mhz~33.45MHz	
VGA_OSC	R387 — TP6(GND)	14.286Mhz~14.925MHz	
24MHz	R114 — TP6(GND)	24.0Mhz±160ppm	
48MHz	R66 — TP6(GND)	48.0Mhz±160ppm	

3.3 POWER switch / FRONT switch check



LED

(1)	POWER
(2)	Hard Disk
(3)	LAN
(4)	Magnetic card reader
(5)	Rest Switch

(1) Using the POWER switch, turned on the power supply.
- Confirm that the system is started and the POWER LED is lit in green.

(2) In the state of (1) above, press the FRONT switch once.
- Confirm that the LCD display is unlit.
- Confirm that the POWER LED is lit in red and the other LEDs are unlit.

(3) In the state of (2) above, press the FRONT switch once again.
- Confirm that the system is started (the same screen as (1) is displayed at the LCD) and the POWER LED is lit in green.

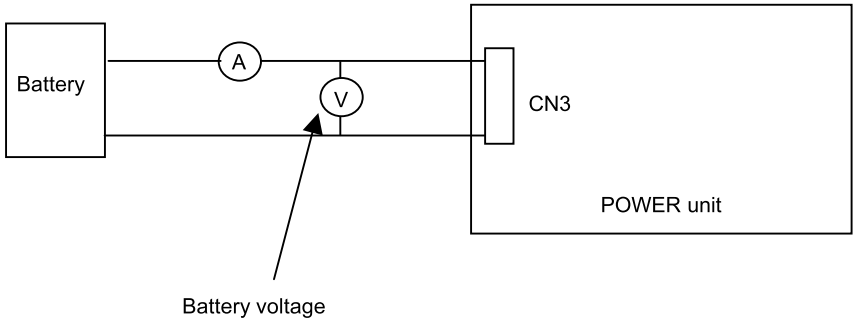
(4) Check rebooting then push the Reset switch.

3.4 Backup function check

1) Measurement of Ni-Cd battery charging current

Standard charging current	Measuring conditions
63mA±15%	Battery voltage: 8.0V

Measurement shall be carried out after the jigs as shown below have been connected. (For reference)



2) Backup operation check

(2) Connect a CRT to the VGA connector and turn on the FCR power supply.

(3) Withdraw from the diagnostic screen. (Press Exit once and return to DOS prompt.)

```
C: >
```

(4) Execute the backup operation check program from DOS prompt.

```
C: >backup   [ENTER] key input
```

(5) When `***** POWER OFF *****` is displayed at the CRT, turn off the AC power supply of the FCR.

(To turn off the AC power supply, the POWER switch is turned off or the AC plug is pulled out.)

(6) Confirm that c:> `***** POWER OFF *****` is displayed at the CRT.

(7) Press the ENTER key once from the keyboard. When the display shown below is presented at the CRT screen, turn on the FCR power supply.

```
C:> ***** POWER OFF *****

Press any key to continue
```

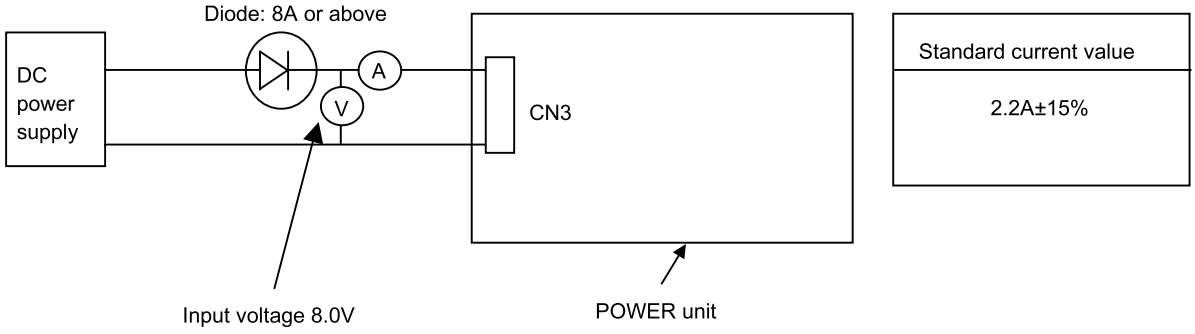
3) Measurement of circuit voltages in backup mode

Measure the voltages specified below in the backup mode by the use of the Ni-Cd battery.

Item	Measuring point	Standard [V]	Remarks
+3V	CN26_8pin - TP6(GND)	+3.3V±0.16	
+5V	CN26_18pin - TP6(GND)	+5.0V±0.25	
+5VSB	CN26_1pin - TP6(GND)	+5.0V±0.25	

4) Measurement of currents in system backup circuit

Measurement shall be carried out after the jigs as shown below have been connected. (For reference)



5) Inspection on the battery voltage detector circuit

(1) Connect the keyboard to the FCR and turn on the power supply. Then finish the diagnostic program. (DOS prompt display)

```
C : >
```

(2) Execute the inspection program for the battery voltage detector circuit.

(3) Apply DC 7.0V from the connected jigs and press an arbitrary key when the following display is presented at the LCD:

```
C : >input voltage = 7.0V

Press any key to continue
```

(4) Confirm that Battery Check = 0 is displayed at the LCD.

```
Input voltage = 7.0V

Press any key to continue

Battery Check = 0
```

(5) In the same manner, apply 7.6V, 8.2V, and 8.5V and examine the battery check value.

Input Voltage	Battery check value
7.0V	0
7.6V	2
8.2V	6
8.5V	7

3.5 Current consumption check

1) Apply the rated voltage that is specified on the main rating plate. The measured current value shall be not greater than the rated current specified on the main rating plate.

3.6 BIOS setup

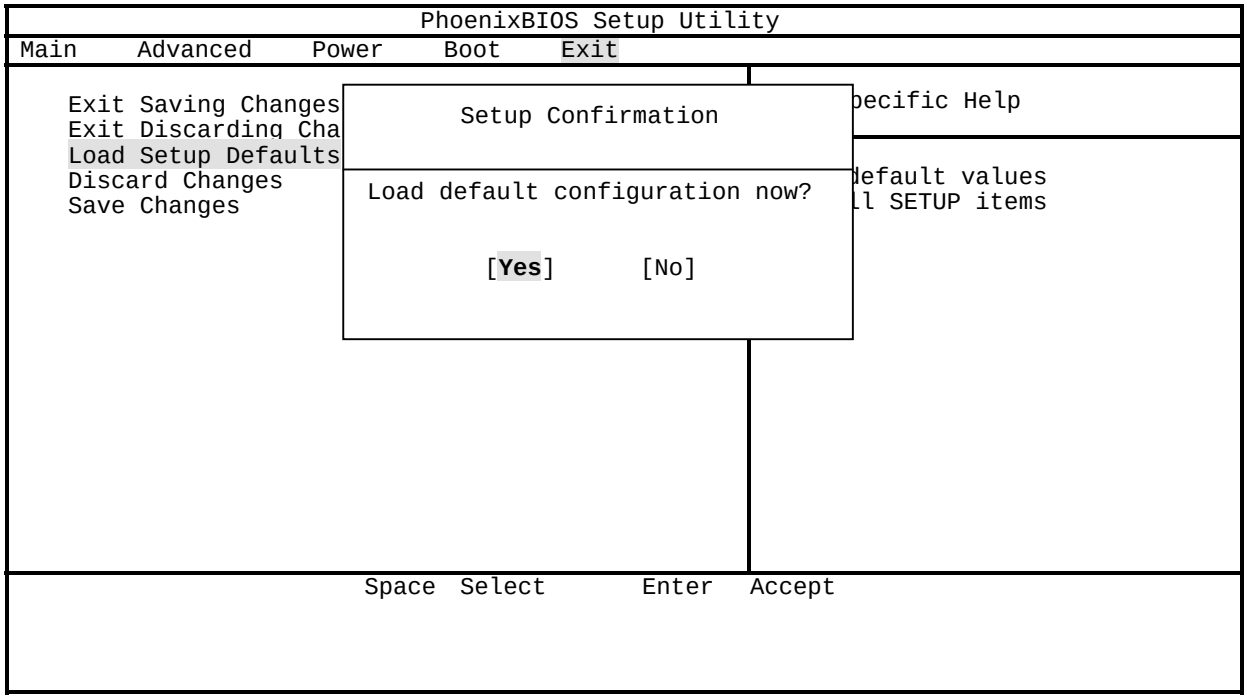
1) Connect the keyboard to the keyboard connector of the JS-170FR, and turn on the POWER switch.

2) When the [DEL] key is pressed in the middle of POST (Power on self test) message display, a screen as shown below is displayed.

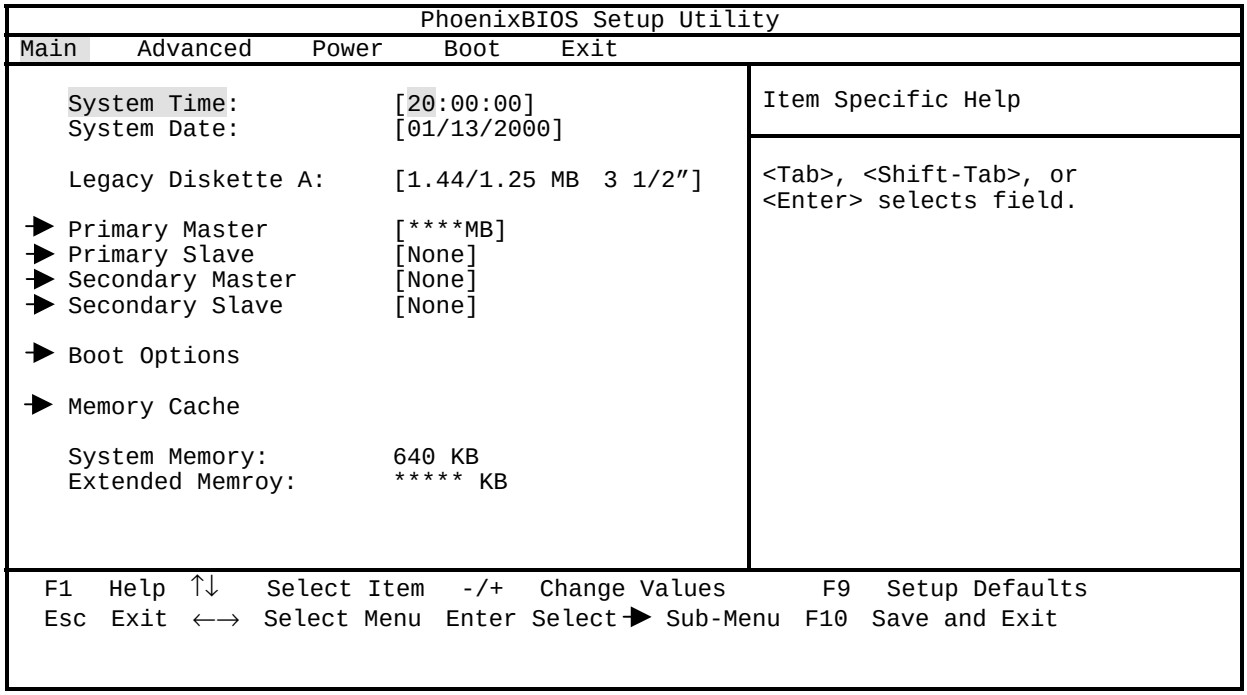
Note) If the BIOS setup is started for the first time, an error message may be presented in the middle of POST message display, according to the initial condition of COMS. However, such a message shall be disregarded.

```
                    PhoenixBIOS Setup Utility
Main    Advanced    Power    Boot    Exit

   System Time:            [xx:xx:xx]          Item Specific Help
   System Date:            [xx/xx/xxxx]
                                    Exit
   Legacy Diskette A:      [1.44/1.25 MB  3 1/2"]  <Tab>, <Shift-Tab>, or
                                                   <Enter> selects field.
 ▶ Primary Master          [****MB]
 ▶ Primary Slave           [None]
 ▶ Secondary Master        [None]
 ▶ Secondary Slave         [None]

 ▶ Boot Options

 ▶ Memory Cache

   System Memory:          640 KB
   Extended Memroy:        ***** KB

  F1   Help ↑↓   Select Item   -/+   Change Values       F9   Setup Defaults
  Esc  Exit ←→   Select Menu  Enter  Select▶ Sub-Menu    F10  Save and
```

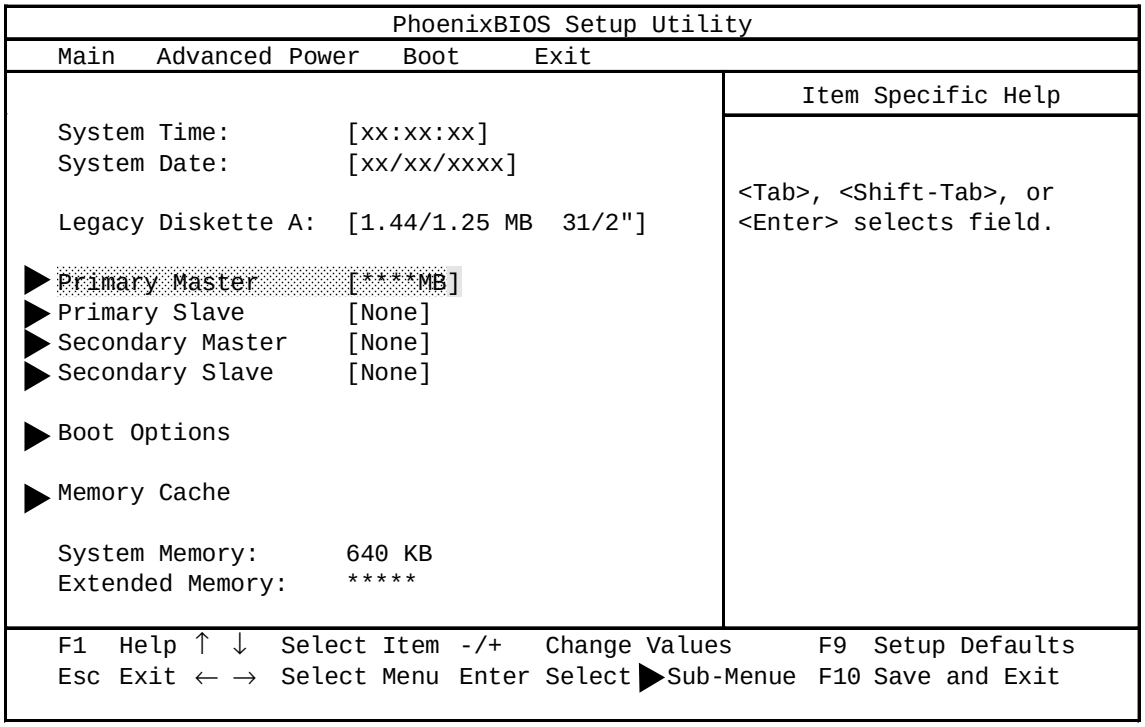
3) Starting from the screen of 2) above, move to "Exit" by means of the rightward arrow mark (→).
Then, using the downward arrow mark (↓), select "Load Setup Defaults" and press the [Enter] key.
A sub-screen is presented as shown below. Then, press the [Enter] key again.



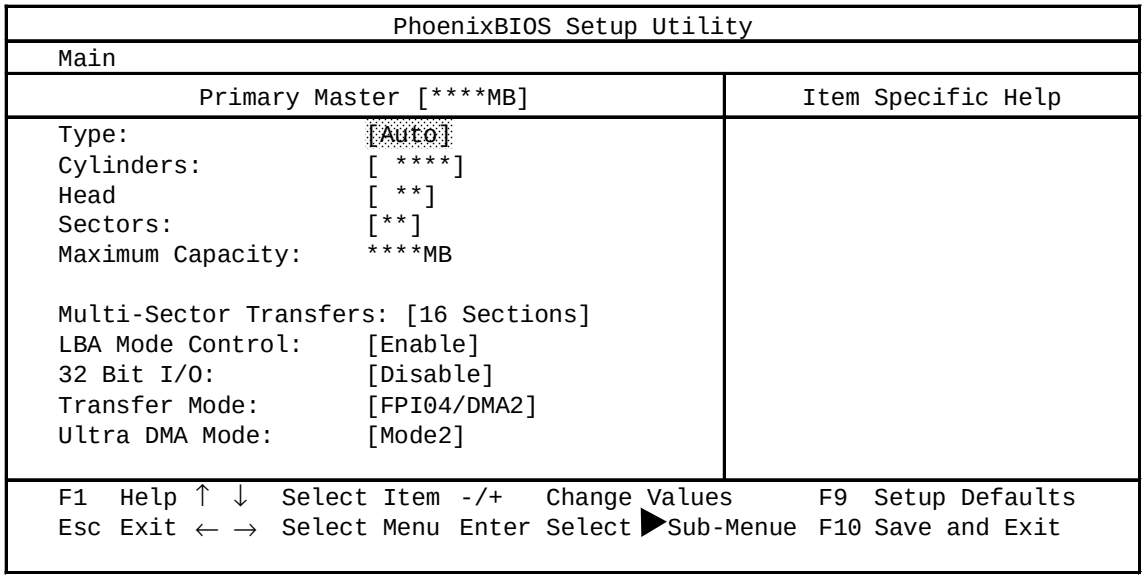
4) Starting from the screen of 3) above, move to "Main" by means of the leftward arrow mark (←).
Then, using the keys of [Tab], [Space], and [↓], set time and data at that time point.
Example) 13 January 2000
20:00


PhoenixBIOS Setup Utility
Main Advanced Power Boot Exit
System Time: [20:00:00]
System Date: [01/13/2000]
Legacy Diskette A: [1.44/1.25 MB 3 1/2"]
Primary Master [****MB]
Primary Slave [None]
Secondary Master [None]
Secondary Slave [None]
Boot Options
Memory Cache
System Memory: 640 KB
Extended Memroy: ***** KB
Item Specific Help
<Tab>, <Shift-Tab>, or
<Enter> selects field.
F1 Help ↑↓ Select Item -/+ Change Values F9 Setup Defaults
Esc Exit ←→ Select Menu Enter Select▶ Sub-Menu F10 Save and Exit

(5)


PhoenixBIOS Setup Utility
Main Advanced Power Boot Exit
Item Specific Help
System Time: [xx:xx:xx]
System Date: [xx/xx/xxxx]
Legacy Diskette A: [1.44/1.25 MB 31/2"]
<Tab>, <Shift-Tab>, or
<Enter> selects field.
Primary Master [****MB]
Primary Slave [None]
Secondary Master [None]
Secondary Slave [None]
Boot Options
Memory Cache
System Memory: 640 KB
Extended Memory: *****
F1 Help ↑ ↓ Select Item -/+ Change Values F9 Setup Defaults
Esc Exit ← → Select Menu Enter Select ▶Sub-Menue F10 Save and Exit

(6) After selecting "Primary Master [****MB]", press the [ENTER] key to enter the "Primary Master" setup screen.


PhoenixBIOS Setup Utility
Main
Primary Master [****MB]
Item Specific Help
Type: [Auto]
Cylinders: [****]
Head [**]
Sectors: [**]
Maximum Capacity: ****MB
Multi-Sector Transfers: [16 Sections]
LBA Mode Control: [Enable]
32 Bit I/O: [Disable]
Transfer Mode: [FPI04/DMA2]
Ultra DMA Mode: [Mode2]
F1 Help ↑ ↓ Select Item -/+ Change Values F9 Setup Defaults
Esc Exit ← → Select Menu Enter Select ▶Sub-Menue F10 Save and Exit

(7) Perform the following steps [1], [2], and [3], on the "Primary Master" setup screen.

[1] Select "Type: [Auto]" by using [↑] or [↓] key on the keyboard, then change the choice to "Type: [User]" by using [-] or [+] key on the keyboard.

[2] Select "Transfer Mode: [FPI04/DMA2]" by using [↑] or [↓] key on the keyboard, then change the choice to "Transfer Mode: [Fast FPI04]" by using [-] or [+] key on the keyboard.

[3] Select "Ultra DMA Mode: [Mode2]" by using [↑] or [↓] key on the keyboard, then change the choice to "Ultra DMA Mode: [Disable]" by using [-] or [+] key on the keyboard.

(8) After performing the steps [1], [2] and [3] above, verify that the setup of "Type:", "Transfer Mode" and "Ultra DMA Mode" appears as follows on the "Primary Master" setup screen.

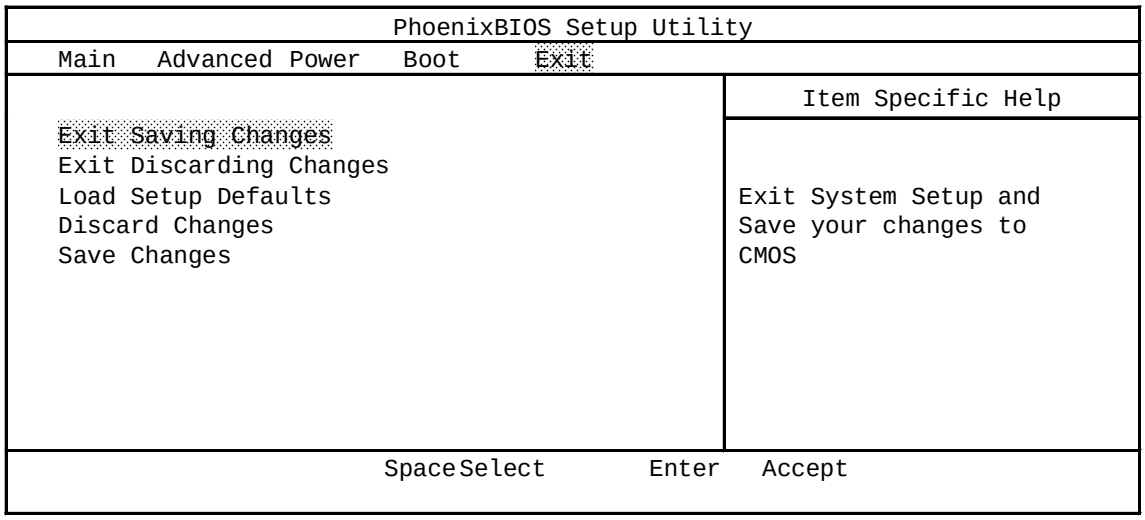
```
Type:    [User]

Transfer Mode:    [Fast PI04]

Ultra DMA Mode:   [Disable]
```

```
                        PhoenixBIOS Setup Utility
  Main
Primary Master [****MB]                          Item Specific Help

  Type:                 [User]
  Cylinders:            [ ****]
  Head                  [ **]
  Sectors:              [**]
  Maximum Capacity:     ****MB

  Multi-Sector Transfers: [16 Sectors]
  LBA Mode Control:     [Enable]
  32 Bit I/O:           [Disable]
  Transfer Mode:        [Fast PI04]
  Ultra DMA Mode:       [Disable]

  F1  Help ↑ ↓  Select Item  -/+   Change Values      F9  Setup Defaults
  Esc Exit ← →  Select Menu  Enter Select ▶Sub-Menue  F10 Save and Exit
```

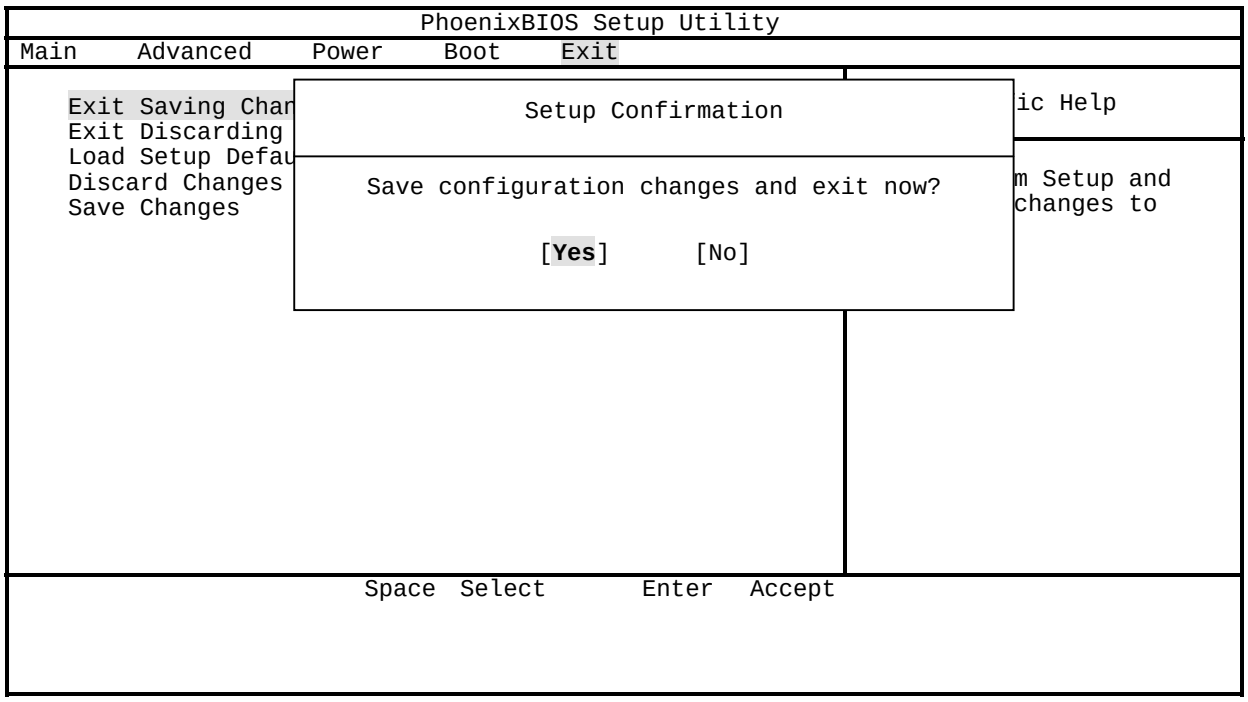
(9) After verifying the setup has been performed correctly, press the [ESC] key on the keyboard to return to the "Main" menu of the "BIOS Setup Utility" screen.

```
                        PhoenixBIOS Setup Utility
  Main   Advanced Power   Boot     Exit
                                                  Item Specific Help
  System Time:          [xx:xx:xx]
  System Date:          [xx/xx/xxxx]

  Legacy Diskette A:    [1.44/1.25 MB  31/2"]

▶ Primary Master        [****MB]
▶ Primary Slave         [None]
▶ Secondary Master      [None]
▶ Secondary Slave       [None]

▶ Boot Options

▶ Memory Cache

  System Memory:        640 KB
  Extended Memory:      ***** KB

  F1  Help ↑ ↓  Select Item  -/+   Change Values      F9  Setup Defaults
  Esc Exit ← →  Select Menu  Enter Select ▶Sub-Menue  F10 Save and Exit
```

(10) Select the "Exit" menu by using [→] or [←] key on the keyboard.



5) Starting from the screen of 4) above, move to "Exit" by means of the rightward arrow mark (→).
Confirm that "Exit Saving Changes" has been selected and press the [Enter] key.
A sub-screen is presented as shown below. Then, press the [Enter] key again.



If automatic restart occurs and a display of "Configuration Error" is presented select "continue" and press the Enter key. Execute the procedures of 3) and thereafter.

3.7 Method of diagnostic program starting

1.Diagnostic Program Start

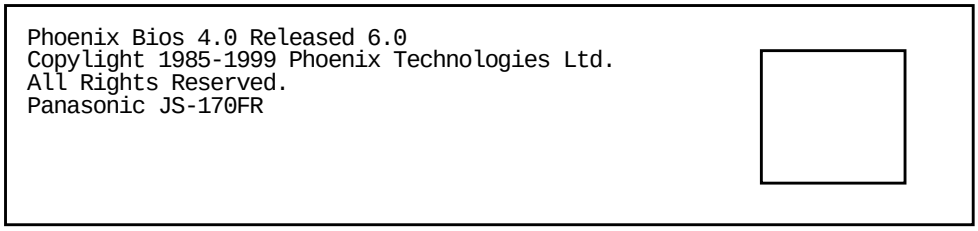
Start the diagnostaic program using a connected keyboard or the touch panel.

With keyboard

1) Connect the keyboard to the keyboard connector, and turn on the POWER switch of the JS-170FR.

2) When the following screen is shown during the starting process, press the [INSERT] key on the keyboard.

LCD DISPLAY

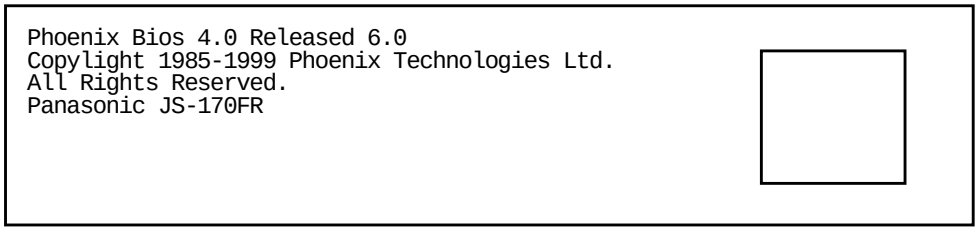


With touch panel (Keyboard not used)

1) Switch the JS-170FR on.

2) When the following screen is shown during the starting process, keep pressing the upper rightcorner of the touch panel.

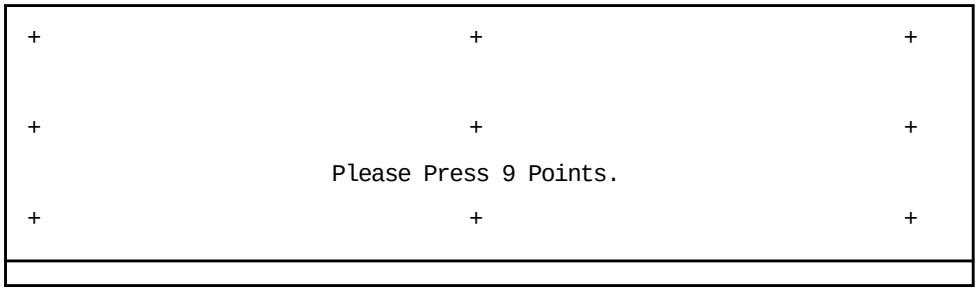
LCD DISPLAY



* A calibration test with the touch panel in the diagnostic program during ROM startup is cleared when turning off the power because its data is not saved.

3) The screen appears as shown below.

LCD DISPLAY

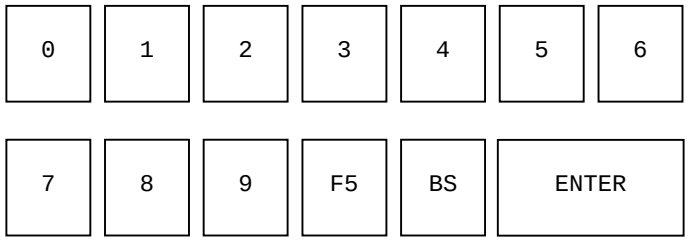


4) Touch each of the nine + points to execute calibration. (A + point disappears from the screen when it is touched.)

5) Confirm that a screen as shown below is displayed at the LCD.

LCD DISPLAY

```
                PANASONIC  JS-170FR TEST  PROGRAM V5.0

  0  : EXIT                          11 : Touch Panel Test.
* 1  : Main Board Test.               12 : Magnetic Card Reader Test.
* 2  : Random Access Memory Test.     13 : Drawer Test.
  3  : Keyboard Test.              *  14 : Inline Test.
  4  : Floppy Disk Test.              15 : Mouse Test.
* 5  : Hard Disk Test.               16 : PCMCIA Test.
* 6  : Video Test.                   17 : Flash Memory Test.
  7  : Parallel Port Test             18 : USB Test.
  8  : Serial Port Test.              19 : Heat Run Test.
  9  : Speaker Test.                  20 : Remote Test.
* 10 : Customer Display Test.

                    Select and Press ENTER Key  :  0_
```



6) Execution of the diagnostic program shall be carried out with the touch panel or the keyboard connected.

3.8 Execution of diagnostic services

1) Main PWB test

(1) Enter "1-ENTER" through the keyboard.

LCD DISPLAY

```
                ***** TEST # 1 Main Board Test. *****

ROM Checksum Test                    OK **/**/**
Shutdown byte read/write Test        OK
PIT Test                             OK
Page register read/write Test        OK
DMA controller Test                  OK
Keyboard Test                        OK
PIC Test                             OK
RTC Test                             OK



Test done press any key.
                                                  EXIT
```

//** : Date of ROM establishment

(2) Finish the test after displaying OK for all the diagnostic items.

(3) Press any key to obtain a menu screen for the diagnostic program.

2) Random Access Memory test

(1) Enter "2-ENTER" through the keyboard.

LCD DISPLAY

```
            ***** TEST # 2 Random Access Memory Test. *****

RAM write/Read Test.
16384  KB  OK.
RAM Address is up to 00FFFFFFH

RAM Refresh Test.
16384  KB  OK.

RAM Address Line Test
RAM Address Bit 23 OK.

Test done. Press any key.

   F1=STOP/ CONTINUE        F2=STOP / MENU

F1=STOP / CONTINUE   F2=STOP / MENU             TEST=RUN
```

(2) Finish the test after checking the RAM capacity and displaying OK for all the diagnostic items.

(3) Press any key to obtain a menu screen for the diagnostic program.

(4) Inspection on a MAIN PWB unit should be carried out for each slot. Otherwise, two DIMM units should be mounted for inspection.

When two 16Mbyte DIMM units are mounted:

RAM size = 32768KB
RAM address = 1FFFFFFH
RAM address bit = 24 bits

When one 64Mbyte DIMM units is mounted:

RAM size = 65536KB
RAM address = 3FFFFFFH
RAM address bit = 25 bits

3) Keyboard test

(1) Connect a PC keyboard to the keyboard connector.

(2) Enter "3-ENTER" through the keyboard.

(3) Select the keyboard type (1: JP, 2: US, 3: GR) and press the Enter key.

LCD DISPLAY

```
                    ***** TEST # 3 Keyboard Test. *****

e 1 2 3 4      5 6 7 8     9 0 1 2 p s p
z 1 2 3 4 5 6 7 8 9 0 - =    b    I h u     n / * -
t Q W E R T Y U I O P    [ ] :   d e d       7 8 9 +
c A S D F G H J K L ; '     e                 4 5 6
s Z X C V B N M , . /         s       ↑       1 2 3 e
c     a         s           a         c ← ↓ →     0   .

Press F1 (OK) or F2 (NG) twice.   OK.
 Test done. Press any key.
```

(4) Display of the key input shall be as specified above.
(However, the lowest line conforms to the keyboard being used.)

(5) When all key inputs have been entered, press the F1 key twice in case of OK or the F2 key in case of NG.

(6) Press any key to obtain a menu screen for the diagnostic program.

4) Floppy Disk test

(1) Prior to turning ON the FCR power supply, connect a 3.5 FDD unit (CF-VFD11) to the FDD connector.

(2) Display a diagnostic menu by the method of 10 described previously.

(3) Set a 3.5" 2HD work diskette (write enabled) in the FDD.

(4) Enter "4-ENTER" through the keyboard.

(5) Press the F1 key to start the test.

LCD DISPLAY

```
                ***** TEST # 4 Floppy Disk Test. *****

Insert a 2HD disk into the Drive
**************  Warning  !!!  **************
CONTENTS OF WILL BE DESTROYED
*****************************************
F1=CONTINUE  F2=MENU

FLOPPY DISK Controller Test             OK
2HD-MEDIA IN 1.44-FDD Test              OK
FLOPPY DISK DRIVE (1.44MFD)Test         OK

Test done. Press any key.

    F1=STOP / CONTINUE      F2=STOP / MENU

          F1=STOP / CONTINUE  F2=STOP / MENU           TEST = RUN
```

(6) Finish the test after displaying OK for all the diagnostic items.

(7) Set a 3.5" 2HD work diskette (write disabled) in the FDD.

(8) Enter "4-ENTER" through the keyboard.

(9) Press the F1 key to start the test.

LCD DISPLAY

```
                ***** TEST # 4 Floppy Disk Test.*****

Insert a 2HD disk into the Drive
**************  Warning  !!!  **************
   CONTENTS OF WILL BE DESTROYED
*****************************************
F1=CONTINUE  F2=MENU

FLOPPY DISK Controller Test                          OK
2HD-MEDIA IN 1.44-FDD Test
Formatting : Cylinder=0 Head=0  Sector=1  Secyor count=18
(03)Write  Protected
FLOPPY DISK DRIVE (1.44MFD)Test                      OK

Test done. Press any key.

  F1=STOP / CONTINUE      F2=STOP / MENU

          F1=STOP / CONTINUE  F2=STOP / MENU           TEST = RUN
```

(10) Finish the test after displaying "(03) Write Protected."

(11) Press any key to obtain a menu screen for the diagnostic program.

5) Hard Disk test

(1) Enter "5-ENTER" through the keyboard.

LCD DISPLAY

```
                ***** TEST # 5 Hard Disk Test. *****

************** Warning !!! **************
 Reserved cylinder for DIAGNOSTICS will lose its data.
 Reserved cylinder number = 787 or (645)
****************************************

Hard DISK CONTROLLER Test       OK
Hard DISK SEEK Test             OK
Hard DISK Read/Write Test       OK
   Reading : Cylinder = 787 or (645) Head = 127 or (239) Sector = 63
   Sector count = 1  When 3.25 GB


Test done. Press any key.

     F1=STOP / CONTINUE    F2=STOP / MENU

          F1=STOP / CONTINUE    F2=STOP / MENU        TEST=RUN
```

(2) Confirm in the middle of testing that the front LED for HDD blinks in green.

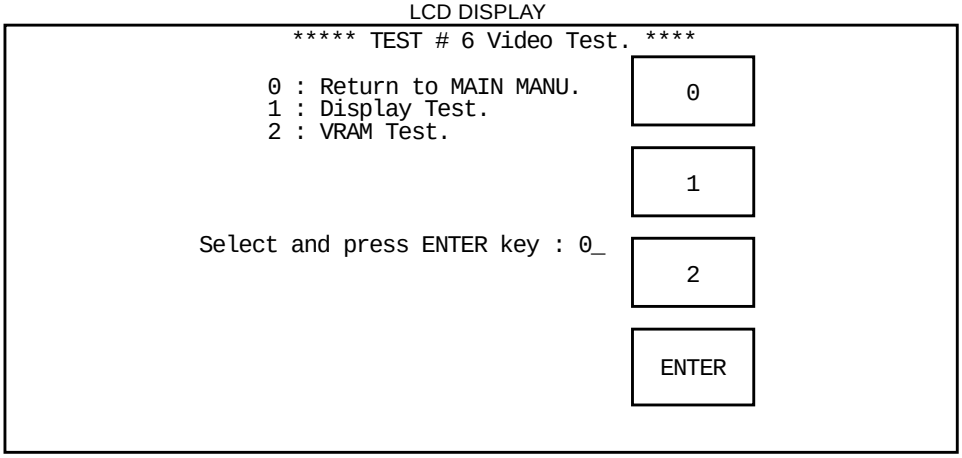
(3) Finish the test after displaying OK for all the diagnostic items.

(4) Press any key to obtain a menu screen for the diagnostic program.

6) Video test

(1) Enter "6-ENTER" through the keyboard.

LCD DISPLAY



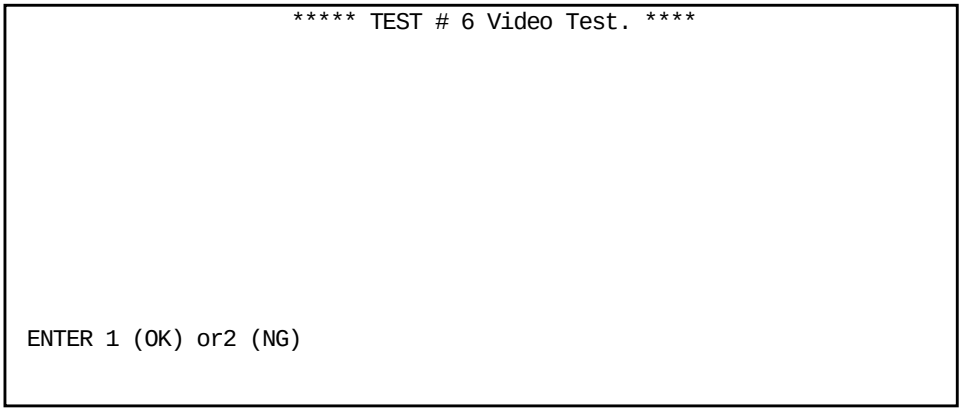
6-1) Display test

(1) Enter "1-ENTER" through the keyboard.

(2) Confirm that the back-lite is turned ON/OFF three times.

(3) Since an all-white screen is displayed, confirm the freedom from any problem, such as dot missing and error display. If the result is OK, press the "1" key. In case of NG, press the "2" key.

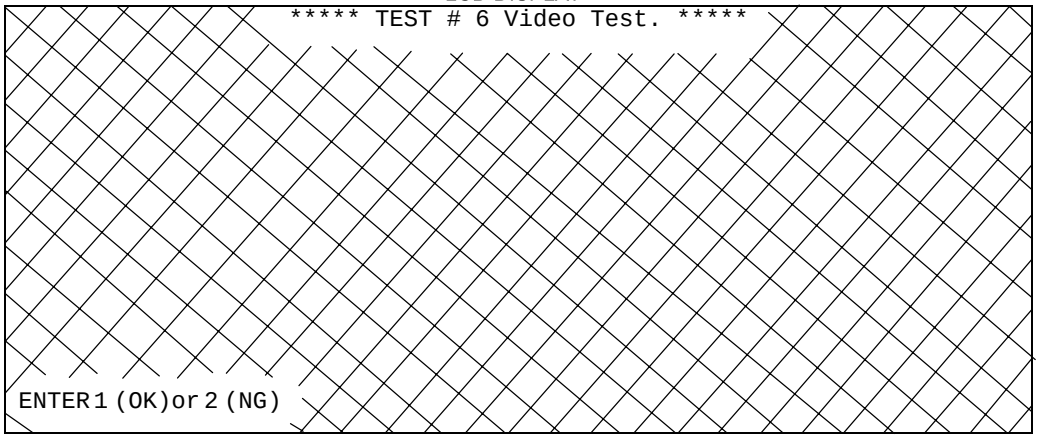
LCD DISPLAY



(4) Since an all-black screen is displayed, confirm the freedom from any problem, such as dot missing and error display. If the result is OK, press the "1" key. In case of NG, press the "2" key.

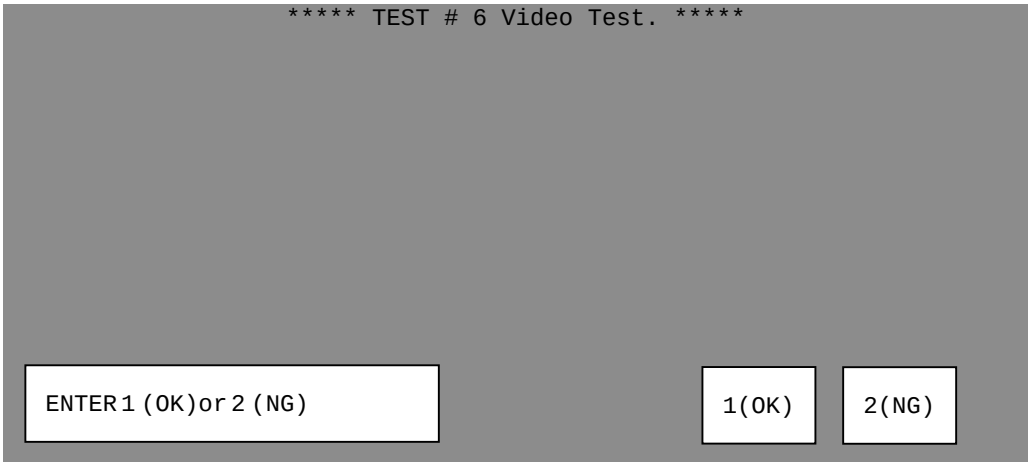
(5) Since a cross hatch screen is displayed, confirm the freedom from any problem, such as distortion, dot missing, and error display. If the result is OK, press the "1" key. In case of NG, press the "2" key.

LCD DISPLAY



(6) Since a checkers pattern screen is displayed, confirm the freedom from any problem, such as dot missing and error display. If the result is OK, press the "1" key. In case of NG, press the "2" key.

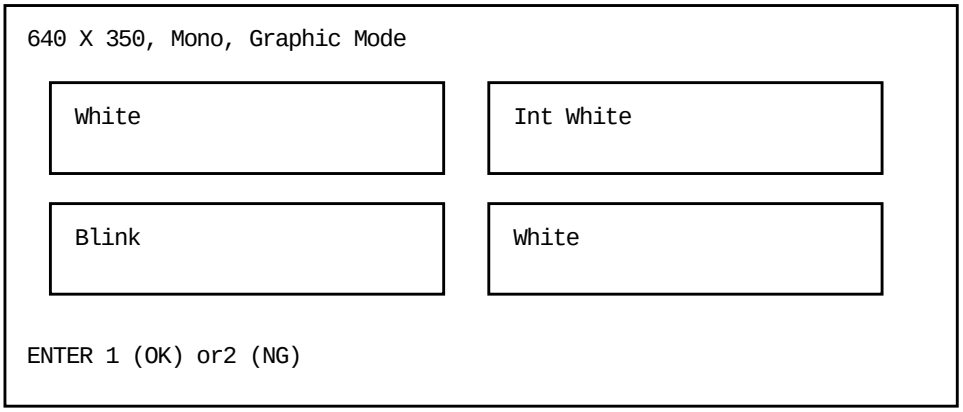
LCD DISPLAY



(7) Since a screen is displayed, of a checkers pattern that is the reverse of the pattern in (6) above, confirm the freedom from any problem, such as dot missing and error display. If the result is OK, press the "1" key. In case of NG, press the "2" key.

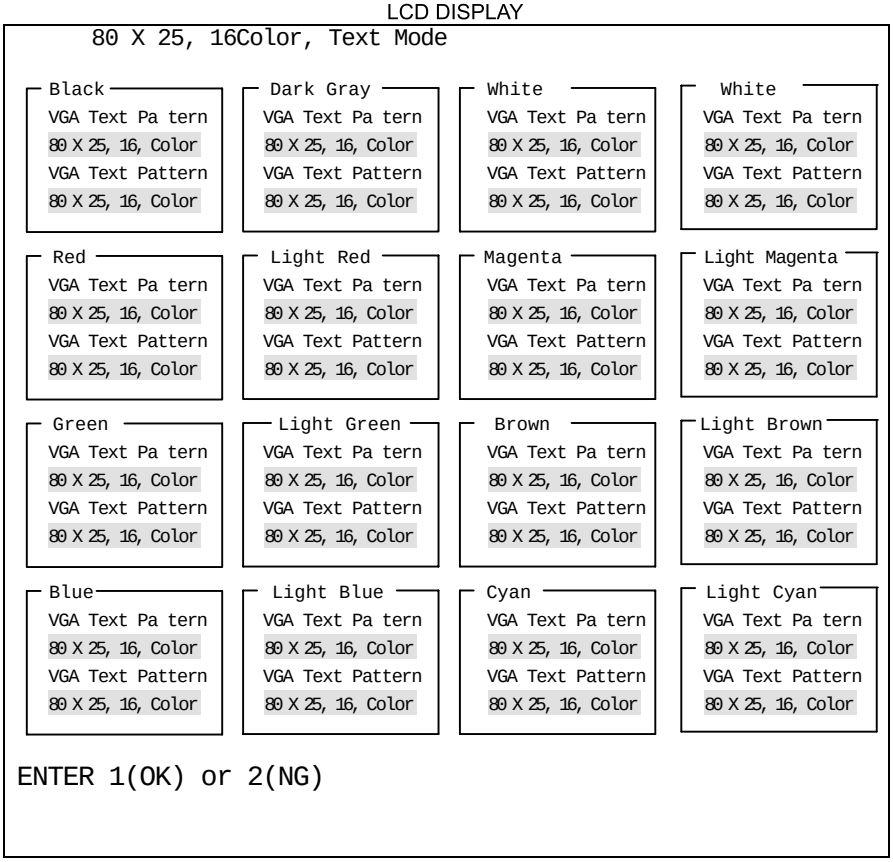
(10) A screen of 640 × 350, Mono, Graphic Mode is displayed. Examine the screen and press the "1" key if the result is OK. Otherwise, press the "2" key.

LCD DISPLAY



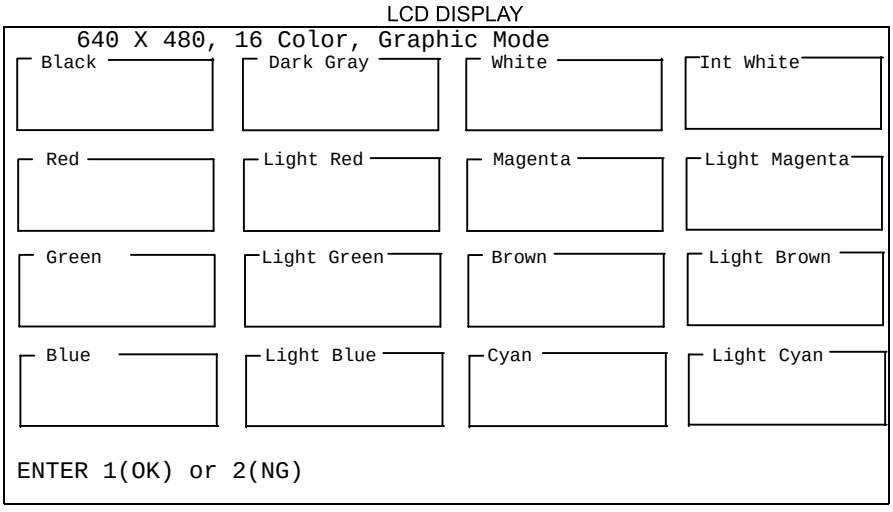
(11) A screen of 80 × 25, 16-Color, Text Mode is displayed. Examine the screen and press the "1" key if the result is OK. Otherwise, press the "2" key. Confirm that the 16 colors are displayed and the actual color is correctly displayed by the character color.(The screened sections keep blinking.)

LCD DISPLAY



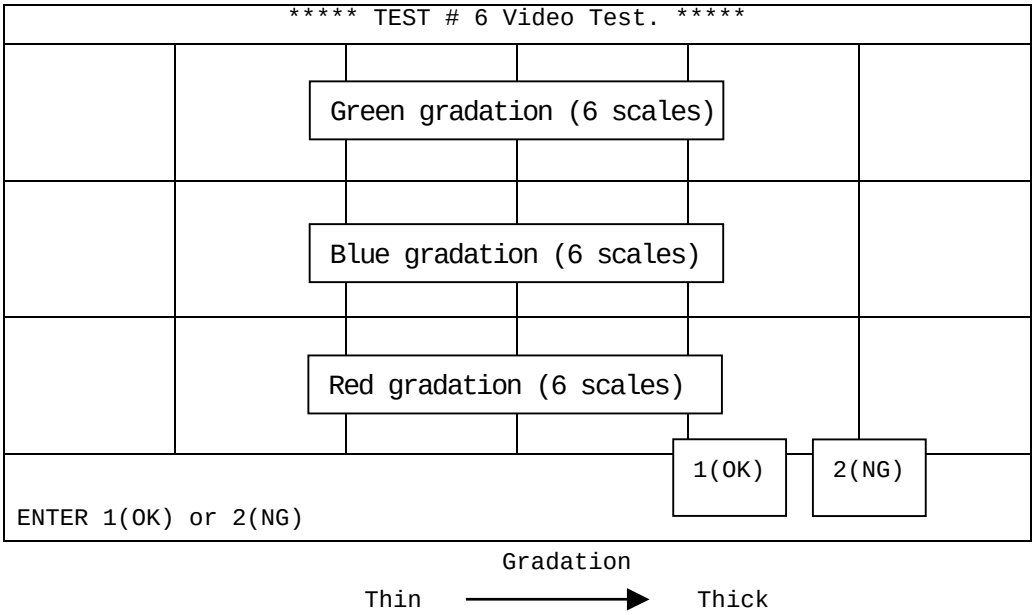
(14) A screen of 640 × 480, 16-Color, Graphic Mode is displayed. Examine the screen and press the "1" key if the result is OK. Otherwise, press the "2" key. Confirm in this case that the 16 colors are actually displayed.

LCD DISPLAY



(15) A gradation of green, blue, and red is displayed. confirm the freedom from decoloration. If the result is OK, press the "1" key. In case of NG, press the "2" key. (Return to #6 Test Menu.)

LCD DISPLAY



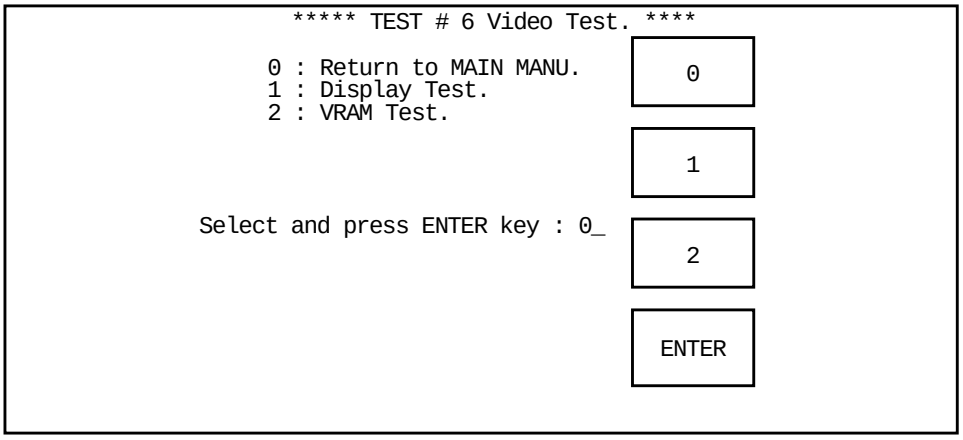
Gradation

Thin ⟶ Thick

6-2) VRAM Test

(1) Enter "2-ENTER" through the keyboard, using the #6 Test Menu.

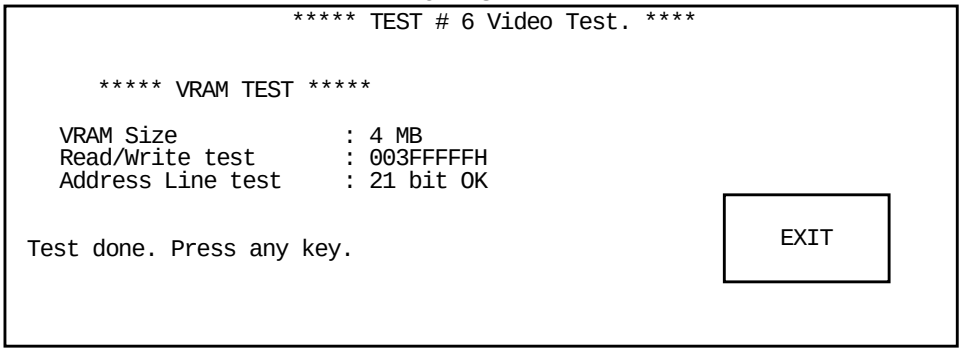
LCD DISPLAY



While the test is carried out, the screen may encounter display turbulence or disappearance.
However, the beep sound generated at the constant intervals indicates that the testing is in progress.

(2) Confirm the display below, which will be presented in the meantime.

LCD DISPLAY


***** TEST # 6 Video Test. ****
***** VRAM TEST *****
VRAM Size : 4 MB
Read/Write test : 003FFFFFH
Address Line test : 21 bit OK
Test done. Press any key.
EXIT

(3) Press any key to recover the #6 Test Menu.

(4) Press "0 - ENTER" key to recover the Main Menu.

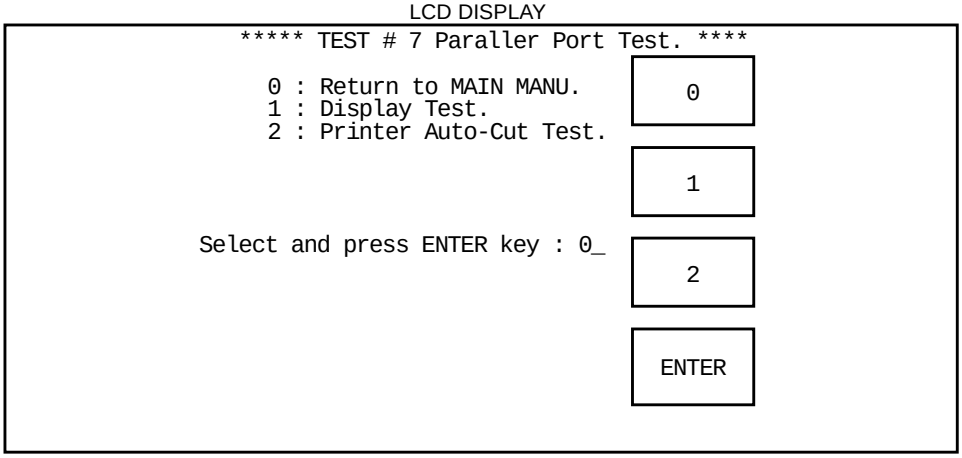
7) Parallel Port test

(1) Connect a printer (TM-300 or TM-T80) to the printer port.
(The lock screw of the printer connector shall be tightened normally.)

(2) Display a diagnostic menu by the method of 10 described previously.

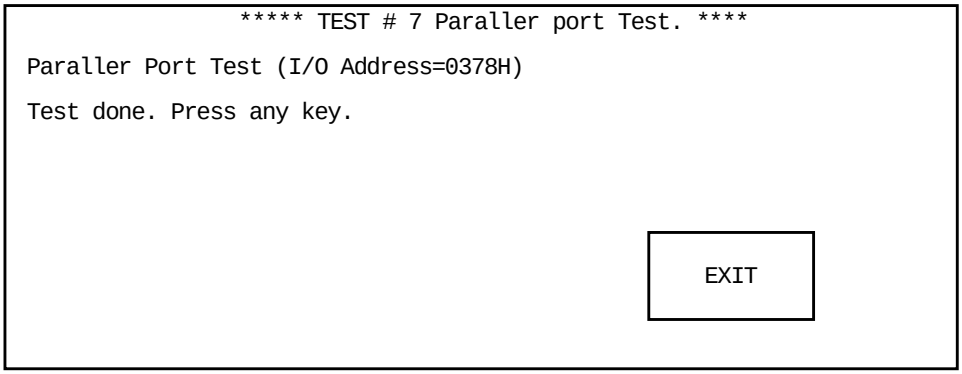
(3) Enter "7-ENTER" through the keyboard.

LCD DISPLAY



(4) Enter "1-ENTER" through the keyboard.

LCD DISPLAY



(The printer begins to print out characters.)
Confirm that the following contents are presented:

i For Printer TM-300

```
Parallel Port test (I/O) Address=0378H)
!"#$%&'()*+,-./0123456789:;<=>?@ABCDEFG
HIJKLMNOPQRRSTUVWXYZ[/]`-`abcdefghijklmno
!"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGH
IJKLMNOPQRRSTUVWXYZ[/]`-`abcdefghijklmnop
"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHI
JKLMNOPQRRSTUVWXYZ[/]`-`abcdefghijklmnopq
#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJ
KLMNOPQRRSTUVWXYZ[/]`-`abcdefghijklmnopqr
$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJK
LMNOPQRRSTUVWXYZ[/]`-`abcdefghijklmnopqrs
%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKL
MNOPQRRSTUVWXYZ[/]`-`abcdefghijklmnopqrst
&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLM
NOPQRRSTUVWXYZ[/]`-`abcdefghijklmnopqrstu
'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMN
OPQRRSTUVWXYZ[/]`-`abcdefghijklmnopqrstuv
()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNO
PQRRSTUVWXYZ[/]`-`abcdefghijklmnopqrstuvw
)*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOP
QRRSTUVWXYZ[/]`-`abcdefghijklmnopqrstuvwx
```

ii For Printer TM-T80

```
Parallel Port test (I/O) Address=0378H)
!"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHI
JKLMNOPQRRSTUVWXYZ[/]`-`abcdefghijklmno
!"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJ
KLMNOPQRRSTUVWXYZ[/]`-`abcdefghijklmnop
"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJK
LMNOPQRRSTUVWXYZ[/]`-`abcdefghijklmnopq
#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKL
MNOPQRRSTUVWXYZ[/]`-`abcdefghijklmnopqr
$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLM
NOPQRRSTUVWXYZ[/]`-`abcdefghijklmnopqrs
%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMN
OPQRRSTUVWXYZ[/]`-`abcdefghijklmnopqrst
&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNO
PQRRSTUVWXYZ[/]`-`abcdefghijklmnopqrstu
'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOP
QRRSTUVWXYZ[/]`-`abcdefghijklmnopqrstuv
()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQ
RRSTUVWXYZ[/]`-`abcdefghijklmnopqrstuvw
)*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQR
STUVWXYZ[/]`-`abcdefghijklmnopqrstuvwx
```

(5) Press any key to obtain the #7 Test screen.

(6) Enter "2-ENTER" through the keyboard. (The printer begins to print out characters. Paper is cut after the completion of printing.)
Confirm that the following contents are presented:

i For Printer TM-300

```
Parallel Port test (I/O) Address=0378H)
!"#$%&'()*+,-./0123456789:;<=>?@ABCDEFG
HIJKLMNOPQRRSTUVWXYZ[/]`-`abcdefghijklmno
!"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGH
IJKLMNOPQRRSTUVWXYZ[/]`-`abcdefghijklmnop
"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHI
JKLMNOPQRRSTUVWXYZ[/]`-`abcdefghijklmnopq
#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJ
KLMNOPQRRSTUVWXYZ[/]`-`abcdefghijklmnopqr
$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJK
LMNOPQRRSTUVWXYZ[/]`-`abcdefghijklmnopqrs
%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKL
MNOPQRRSTUVWXYZ[/]`-`abcdefghijklmnopqrst
&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLM
NOPQRRSTUVWXYZ[/]`-`abcdefghijklmnopqrstu
'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMN
OPQRRSTUVWXYZ[/]`-`abcdefghijklmnopqrstuv
```

Cut in this position

```
?@ABCDEFGHIJKLMNOP
```

ii For Printer TM-T80

```
Parallel Port test (I/O)  Address=0378H)
 !"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHI
JKLMNOPQRRSTUVWXYZ[/]`-`abcdefghijklmno
!"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJ
KLMNOPQRRSTUVWXYZ[/]`-`abcdefghijklmnop
"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJK
LMNOPQRRSTUVWXYZ[/]`-`abcdefghijklmnopq
#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKL
MNOPQRRSTUVWXYZ[/]`-`abcdefghijklmnopqr
$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLM
NOPQRRSTUVWXYZ[/]`-`abcdefghijklmnopqrs
%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMN
OPQRRSTUVWXYZ[/]`-`abcdefghijklmnopqrst
&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNO
PQRRSTUVWXYZ[/]`-`abcdefghijklmnopqrstu
'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOP
QRRSTUVWXYZ[/]`-`abcdefghijklmnopqrstuv
()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQ
RRSTUVWXYZ[/]`-`abcdefghijklmnopqrstuvw
)*+,-./0123456789:;<=>

QRRSTUVWXYZ[/]`-`abcdefghijklmnopqrstuvwx
```

Cut here.

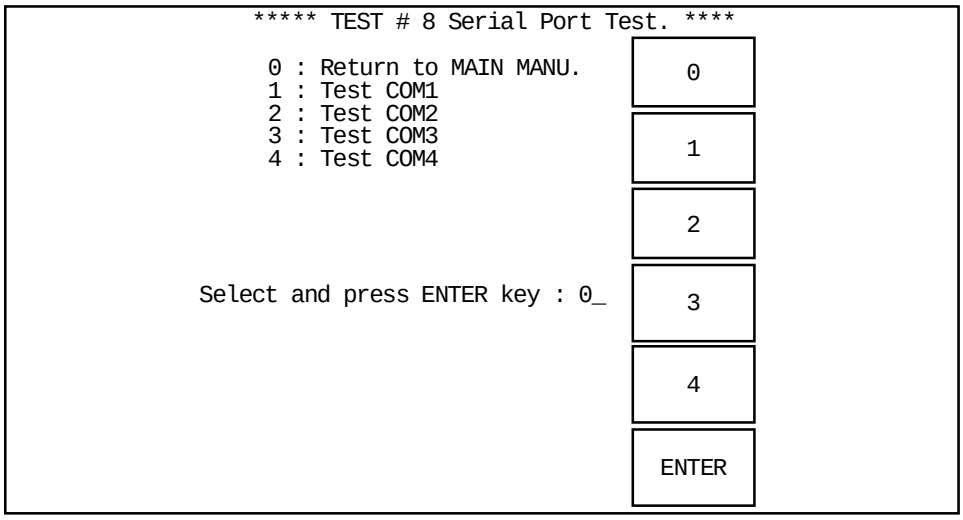
(7) Press any key to obtain the #7 Test screen.

(8) Enter "0-ENTER" through the keyboard to obtain a menu screen for the diagnostic program.

8) Serial Port test

(1) Enter "8-ENTER" through the keyboard.

LCD DISPLAY



(2) No testing is carried out for the item of 4: Test COM 4.

8-1) COM1 test

(1) Connect a loopback connector to the COM1 port.
(The lock screw of the loopback connector shall be tightened normally.)

(2) Enter "1-ENTER" through the keyboard.

LCD DISPLAY

```
                ***** TEST # 8 Serial port Test. ****

   Test COM1 (I/O Address 03F8H)

RS232C Controller Register R/W Test          OK
INTERNAL LOOPBACK Test                       OK
EXTERNAL LOOPBACK Test                       OK


   Test done. Press any key.


                                              EXIT
```

(3) Finish the test after displaying OK for all the diagnostic items.

(4) Press any key to obtain the #8 Test screen.

(5) Disconnect the loopback connector that has been connected to the COM1 port.

(6) Enter "1-ENTER" through the keyboard.

LCD DISPLAY

```
                ***** TEST # 8 Serial port Test. ****

    Test COM1 (I/O Address 03F8H)

RS232C Controller Register R/W Test          OK
INTERNAL LOOPBACK Test                       OK
EXTERNAL LOOPBACK Test
CD ERROR
CTS ERROR
    Test done. Press any key.


                                              EXIT
```

(7) The "EXTERNAL LOOPBACK Test" shall result in "CD ERROR" and "CTS ERROR."

(8) Press any key to obtain the #8 Test screen.

8-2) COM2 test

(1) Connect a loopback connector to the COM2 port.
(The lock screw of the loopback connector shall be tightened normally.)

(2) Enter "2-ENTER" through the keyboard.

LCD DISPLAY

```
                ***** TEST # 8 Serial port Test. ****

  Test COM2 (I/O Address 02F8H)

RS232C Controller Register R/W Test         OK
INTERNAL LOOPBACK Test                      OK
EXTERNAL LOOPBACK Test                      OK


  Test done. Press any key.


                                              EXIT
```

(3) Finish the test after displaying OK for all the diagnostic items.

(4) Press any key to obtain the #8 Test screen.

(5) Disconnect the loopback connector that has been connected to the COM2 port.

(6) Enter "2-ENTER" through the keyboard.

LCD DISPLAY

```
                ***** TEST # 8 Serial port Test. ****

  Test COM2 (I/O Address 02F8H)

RS232C Controller Register R/W Test         OK
INTERNAL LOOPBACK Test                      OK
EXTERNAL LOOPBACK Test
CD ERROR
CTS ERROR
  Test done. Press any key.


                                              EXIT
```

(7) The "EXTERNAL LOOPBACK Test" shall result in "CD ERROR" and "CTS ERROR."

(8) Press any key to obtain the #8 Test screen.

8-3) COM3 test

(1) Connect a loopback connector to the COM3 port.
(The lock screw of the loopback connector shall be tightened normally.)

(2) Enter "3-ENTER" through the keyboard.

LCD DISPLAY

```
                ***** TEST # 8 Serial port Test. ****

  Test COM3 (I/O Address 3220H)

RS232C Controller Register R/W Test          OK
INTERNAL LOOPBACK Test                       OK
EXTERNAL LOOPBACK Test                       OK


  Test done. Press any key.

                                              EXIT
```

(3) Finish the test after displaying OK for all the diagnostic items.

(4) Press any key to obtain the #8 Test screen.

(5) Disconnect the loopback connector that has been connected to the COM3 port.

(6) Enter "3-ENTER" through the keyboard.

LCD DISPLAY

```
                ***** TEST # 8 Serial port Test. ****

  Test COM3 (I/O Address 3220H)

RS232C Controller Register R/W Test          OK
INTERNAL LOOPBACK Test                       OK
EXTERNAL LOOPBACK Test                       OK
CTS ERROR

  Test done. Press any key.

                                              EXIT
```

(7) The "EXTERNAL LOOPBACK Test" shall result in "CTS ERROR."

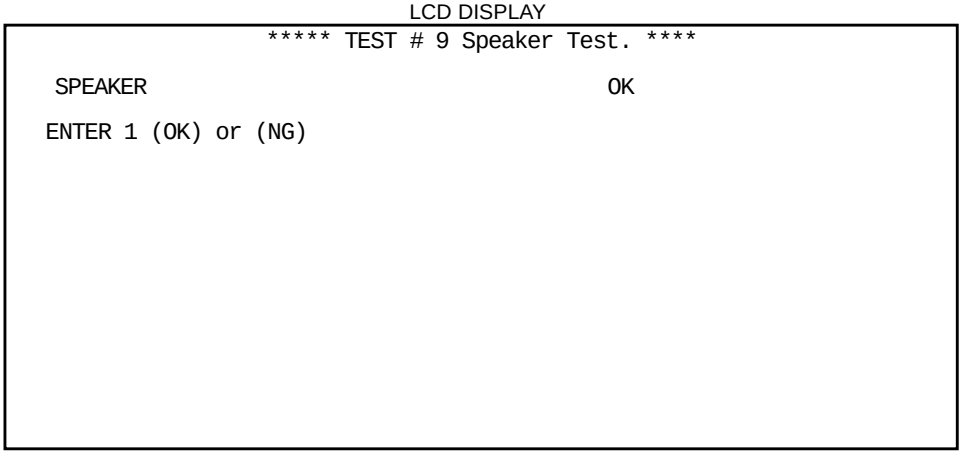
(8) Press any key to obtain the #8 Test screen.

(9) Enter "0-ENTER" through the keyboard to obtain a menu screen for the diagnostic program.

9) Speaker test

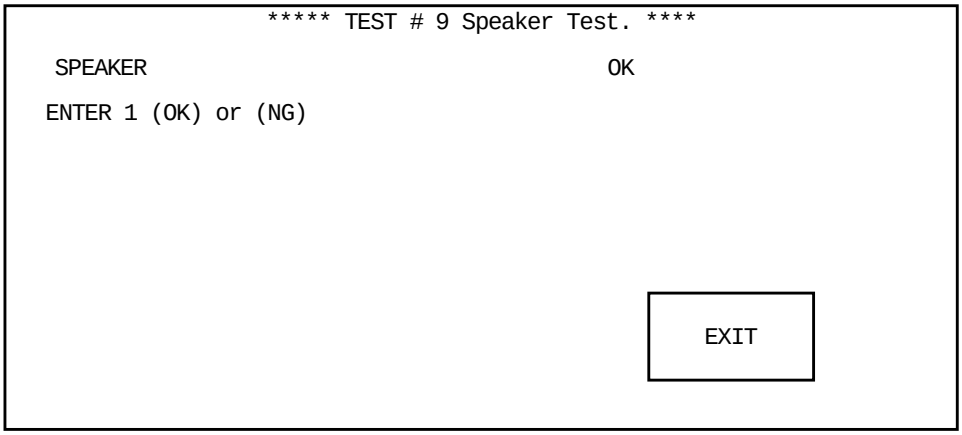
(1) Enter "9-ENTER" through the keyboard.

LCD DISPLAY



(2) If the buzzer tone is confirmed, press the "1" key.

LCD DISPLAY

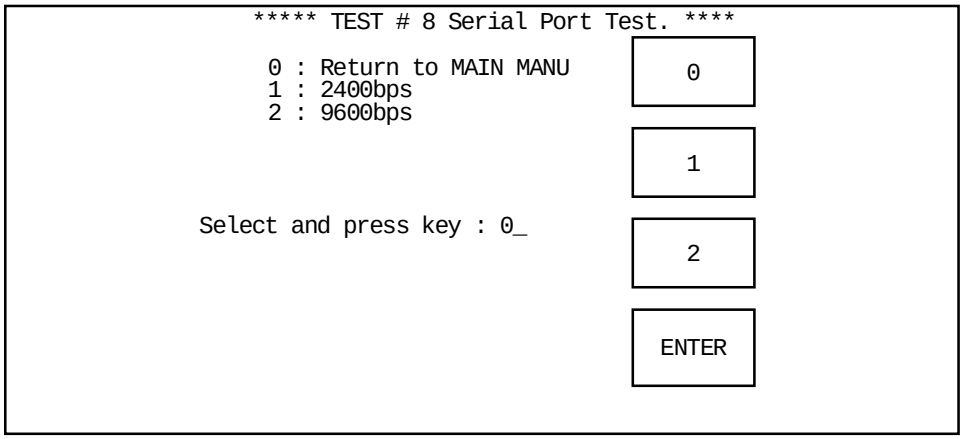


(3) Press any key to obtain a menu screen for the diagnostic program.

10) Customer Display Test

(1) Enter "10-ENTER" though the keyboard

LCD DISPLAY



For JS-170FR-G**, select "1: 2400bps".
For a model other than JS-170FR-G**, select "2: 9600bps".

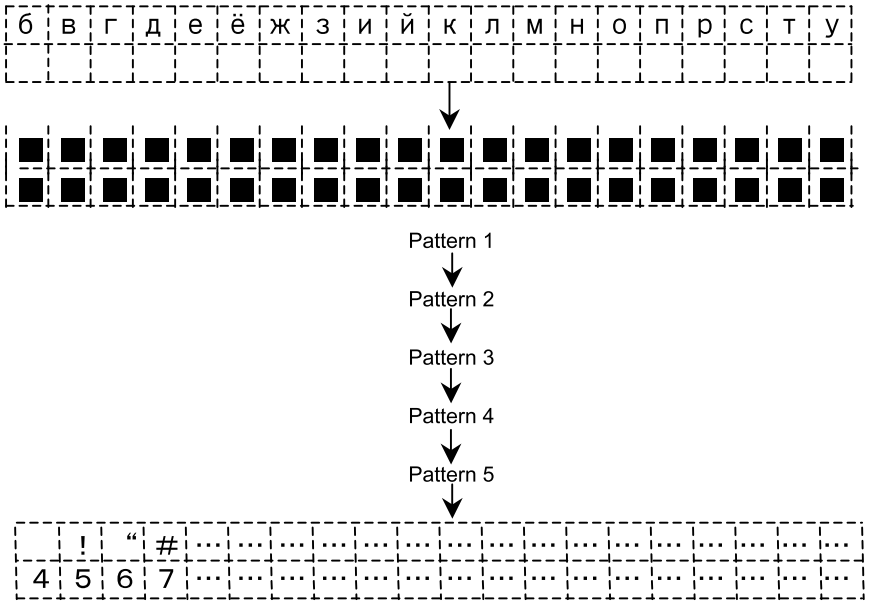
11) Customer Display test

(1) Enter "10-ENTER" through the keyboard.

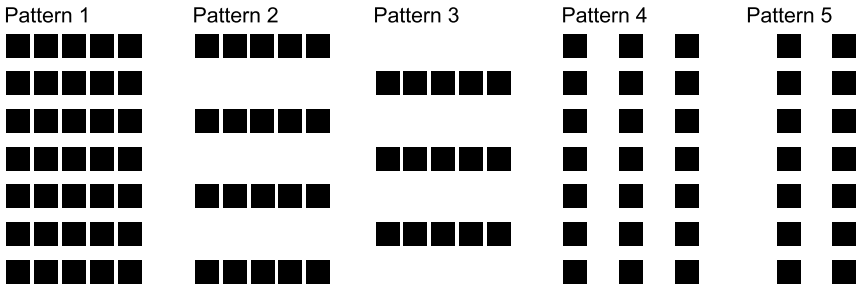
LCD DISPLAY

```
          ***** TEST # 10 Customer Display Test. ****

 CUSTMER DISUPLAY                          OK

 ENTER 1 (OK) or (NG)
 Test done. Press any key.




    F1=STOP/CONTINUE F2=STOP/MENU              TEST=RUN
```

(2)



(3) Press any key to obtain a menu screen for the diagnostic program.

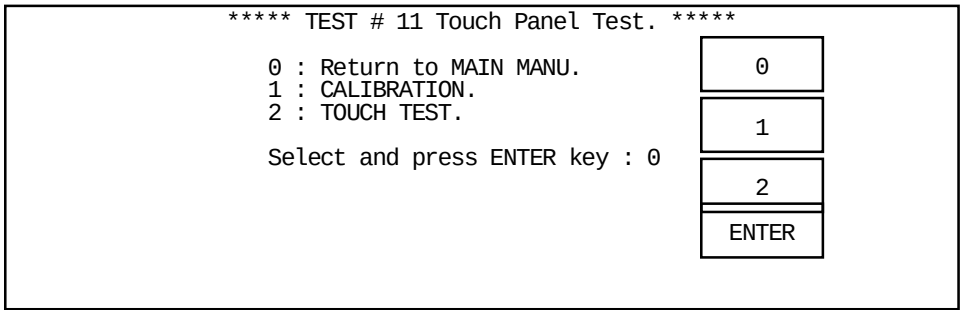


Note) The Customer Display is not mounted on the JS-170FR-*21 (*: E, G, A, W, U, S, F, C). Therefore, this test shall be carried out only in the case of PWB inspection.

12) Touch Panel test

(1) Enter "11-ENTER" through the keyboard.

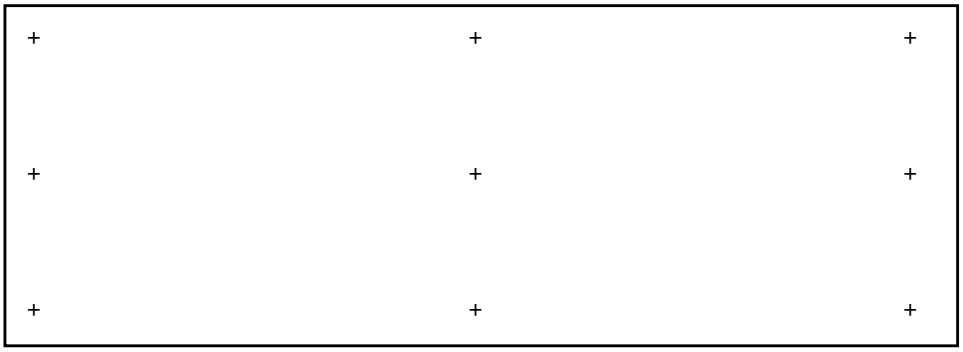
LCD DISPLAY



12-1)Touch panel calibration

(1) Enter "1-ENTER" through the keyboard to perform the calibration test.

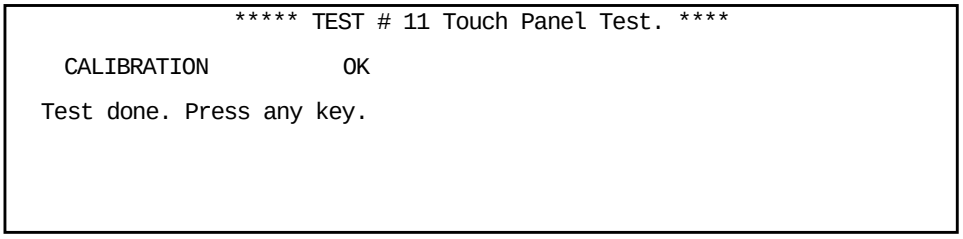
LCD DISPLAY



(2) Touch the center of each + mark (9 points) to perform calibration.
(The + mark disappears from the screen when it is touched.)
If it is necessary to stop the testing work as a result of touching a wrong point by mistake during calibration, touch all the nine points to withdraw from the calibration screen. Since then, restart the test from the step of (2) above.

(3) Upon normal completion of calibration, the following screen display is presented:

LCD DISPLAY



If "CALIBRATION NG" is displayed, restart the test from the step of (2) above.

(4) Press any key to recover the screen of [***** TEST #11 Touch Panel Test.*****].

12-2) Touch Panel test

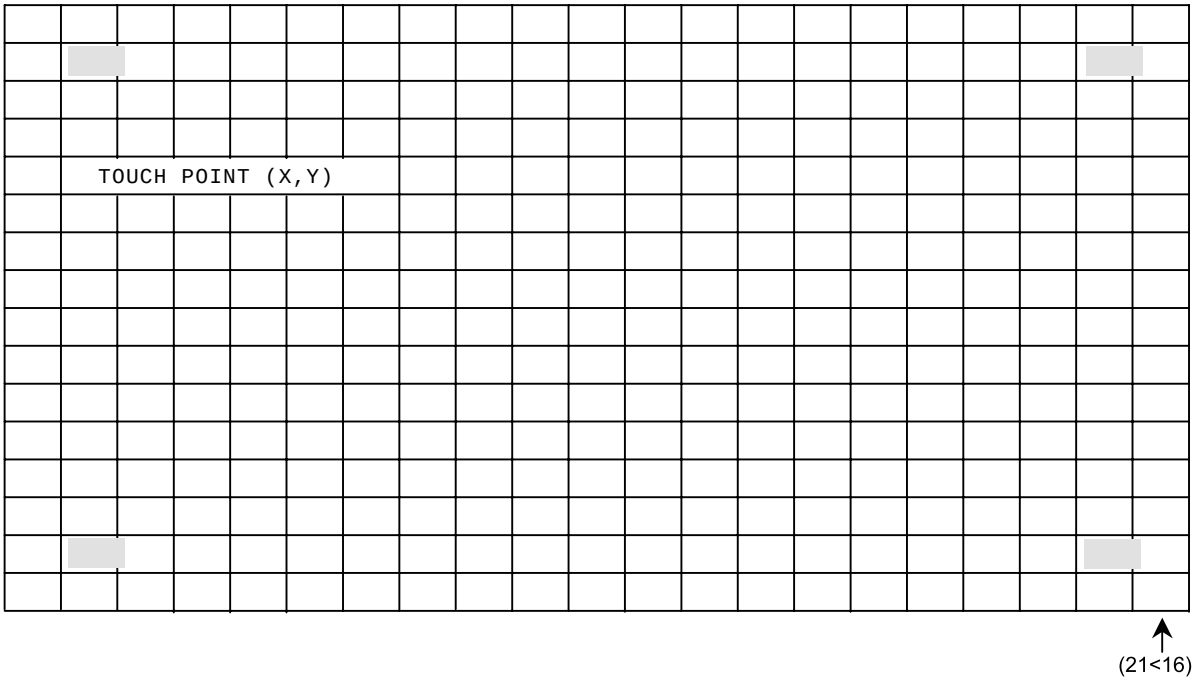
LCD DISPLAY

```
***** TEST # 11 Touch Panel Test. *****

   0 : Return to MAIN MANU.
   1 : CALIBRATION.
   2 : TOUCH TEST.

   Select and press ENTER key : 0
```

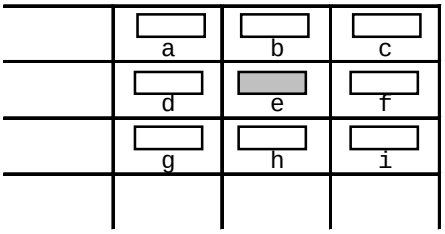
0
1
2
ENTER

(1) Enter "2-ENTER" through the keyboard to perform the Touch test.

LCD DISPLAY



(2) In the all-item touch-panel test screen, the test shall be carried out on the screened keys of (2,2), (2,15), (11,8), (20,2), and (20,15). Judgment of OK/NG shall conform to the example shown below.
The condition shall be regarded as OK if the keys "a, b, c, d, f, g, h, i" do not show any reaction (black & white reversed in the screen) when the area in the inner frame of the "e" key (hatched area) is touched.



(3) Press (21,16) to recover the screen of [***** TEST #11 Touch Panel Test.*****].

LCD DISPLAY

```
            ***** TEST # 11 Touch Panel Test. *****

   2. TOUCH TEST      OK

   ENTER 1 (OK) or (NG)
Test done. Press any key._
```

(4) Enter "0-ENTER" through the keyboard to obtain the test program screen.

(5) Select "Primary Master [****MB]" by using [↑] or [↓] key on the keyboard.

Note: "NG" is shown as a result of the calibration test with the touch panel for a model onto which the application has not been installed. Accordingly, determination whether the result of the calibration test is OK or NG should be made according to the touch panel test after the calibration test.

Calibration: OK = Touch panel test: OK

Calibration: NG = Touch panel test: NG

The calibration data is cleared when turning off the power because the data is not saved on the disk.

13) Magnetic Card test

(1) Prior to turning ON the FR power supply, connect a magnetic card reader unit (JS-140MG-XXX or JS-170MG-010).

(2) Turn on the power supply and confirm that the LED for the magnetic card is lit in green.

(3) Enter "12-ENTER" through the keyboard.

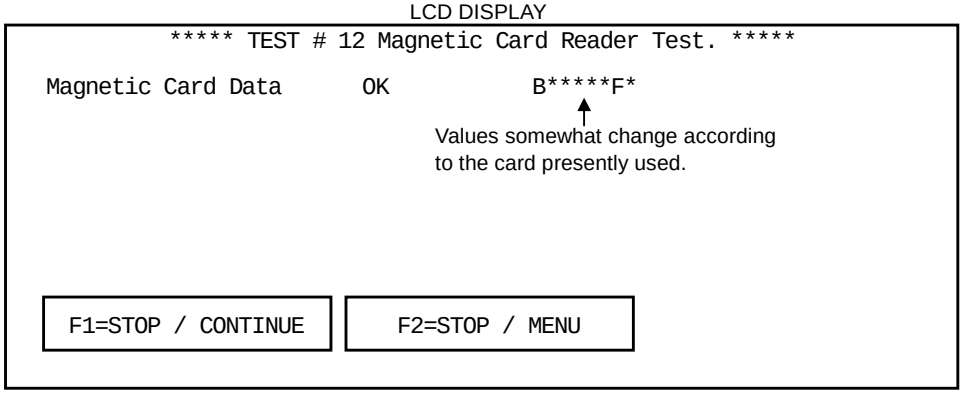
(4) Let the magnetic card reader unit read out a card in the reverse direction and confirm that the LED for the magnetic card is lit in red.

(5) Let the magnetic card reader unit read out a card in the forward direction and confirm that the LED for the magnetic card is not lit in red. Confirm also that the card data are correctly displayed on the screen.

When the JS-140MG is used (JIS1 track 2/ISO2 card is used.)
Main PWB SW1 setting

1	2	3	4	5	6
—	—	ON	ON	ON	ON

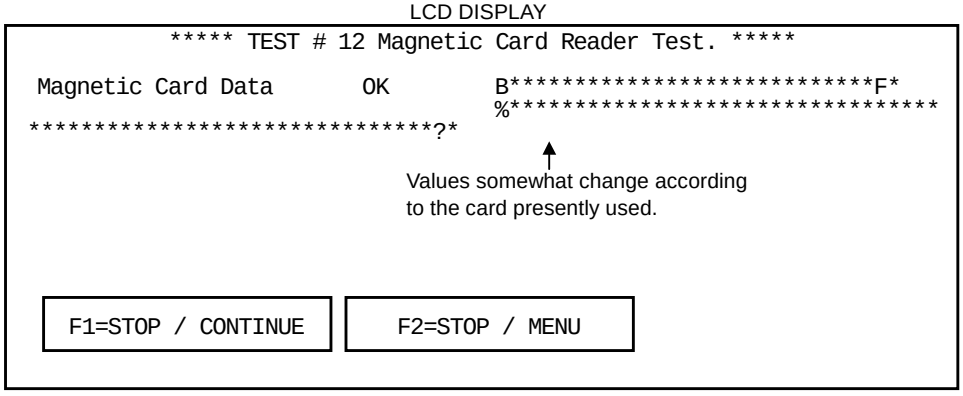
LCD DISPLAY


***** TEST # 12 Magnetic Card Reader Test. *****
Magnetic Card Data OK B*****F*
Values somewhat change according to the card presently used.
F1=STOP / CONTINUE
F2=STOP / MENU

When the JS-170MG is used (JIS1 track 2/ISO2 card + JIS1 track 1/ISO1 card are used)
Main PWB SW1 setting

1	2	3	4	5	6
—	—	ON	OFF	ON	ON

LCD DISPLAY


***** TEST # 12 Magnetic Card Reader Test. *****
Magnetic Card Data OK B**********F*
%**********
**********?*
Values somewhat change according to the card presently used.
F1=STOP / CONTINUE
F2=STOP / MENU

(6) When the OK sign is perceived, press any key to obtain a menu screen for the diagnostic program.
Confirm that the LED is lit in orange when the magnetic card reader unit is disconnected and the power supply is turned on.

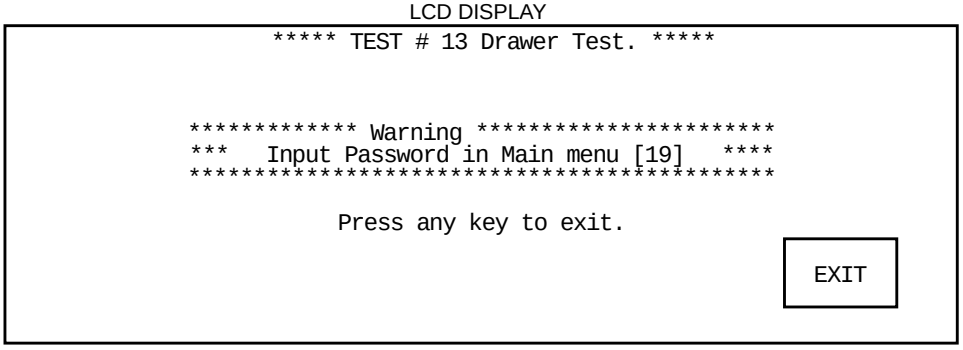
LED color	Lighting conditions
Green	(1) In the state that the card reader is incorporated and the card can be read out. (Lit in green when the power supply is ON.)
	(2) In the state that the card is correctly read out. (The LED is not lit while the card is being read out.)
Red	(1) In the state that the card reader is incorporated and the card can be read out.
	(2) In the state that the card is not correctly read out. (The LED is not lit while the card is being read out.)
	(3) When the card is read out in the reverse direction.
Orange	(1) In the state that the card reader is not incorporated and the card cannot be read out.

(7) Press the F2 key test program to obtain the test program screen.

Note) If the buzzer sounds during testing, try to repeat the test again.
After the completion of testing, return the DIP switches to their original positions.

In the initialized state, the drawer test is locked by the password. If the screen appears as shown below, execute No.19 [Input PASSWORD], and execute the drawer test again.

LCD DISPLAY

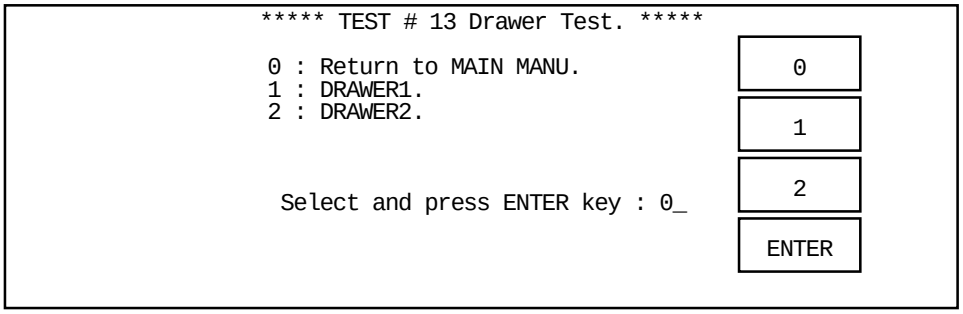


14) Drawer test

(1) Connect a drawer (JS-170CD) to the DRAWER connector.

(2) Enter "13-ENTER" through the keyboard.

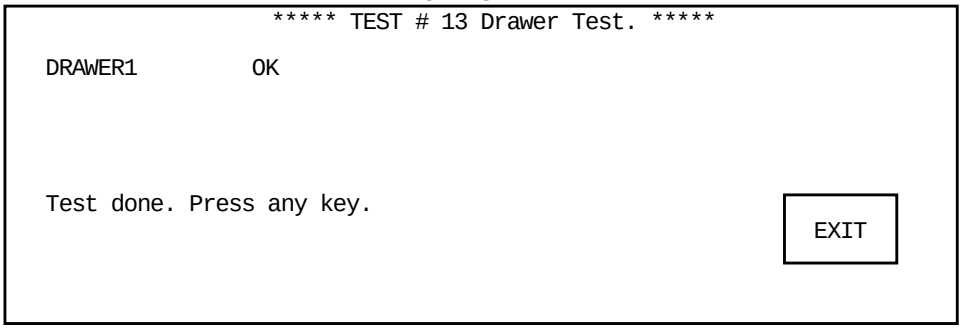
LCD DISPLAY



(3) Enter "13-ENTER" through the keyboard. (At that time, the drawer shall be connected to DRAWER 1.)

(4) Confirm that the drawer is open.

LCD DISPLAY



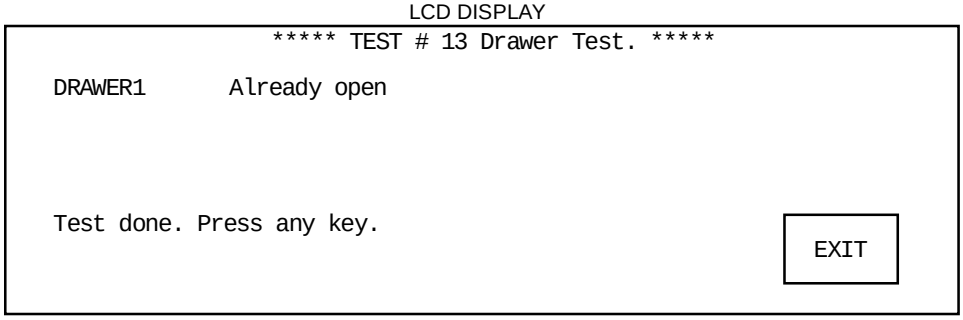
(5) Finish the test when the OK sign is perceived.

(6) Press any key to obtain the #13 Test Menu screen.

(7) Maintain the condition that the drawer is open.

(8) Enter "1-ENTER" through the keyboard.

LCD DISPLAY



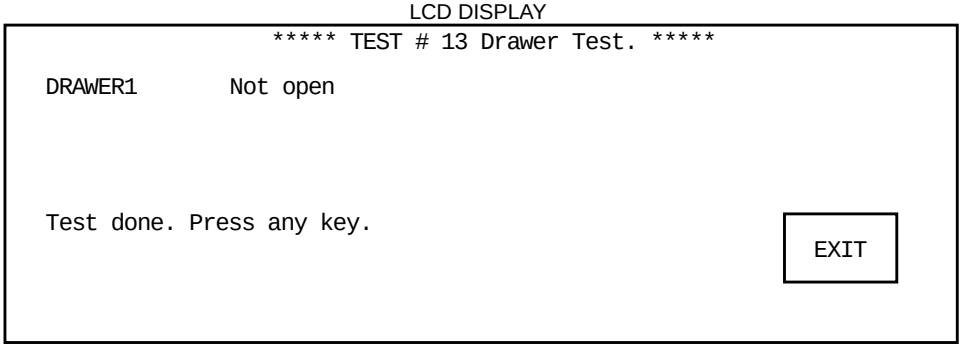
(9) Check the display of "Already open" and finish the test.

(10) Press any key to obtain the #13 Test Menu screen.

(11) Maintain the condition that the drawer is closed.
Hold the front section of the drawer by hand to prevent it from opening.

(12) Enter "1-ENTER" through the keyboard.

LCD DISPLAY



(13) Check the display of "Not open" and finish the test.

(14) Press any key to obtain the #13 Test Menu screen.

(15) Enter "0-ENTER" through the keyboard to obtain the test program screen.

15) Inline test

15-1) LAN-ID setting

(1) Enter "14-ENTER" through the keyboard.

LCD DISPLAY

```
***** TEST # 14 Inline Test. *****

  0 : Return to MAIN MANU
  1 : Set Configutation
  2 : Send Data
  3 : Receive Data
  4 : Self Test


Select and press ENTER key : 0
```

(2) Enter "1-ENTER" through the keyboard. (For Set Configuration, only keyboard can be operated.)

LCD DISPLAY

```
***** TEST # 14 Inline Test. *****

0 : EXIT
1 : Ethernet Address ************
2 : Set EEPROM



Select and press ENTER key : 0
```

(3) Enter "1-ENTER" through the keyboard.

LCD DISPLAY

```
***** TEST # 14 Inline Test. *****

 Ethernet Address Set

               1234567890AB

Set and press ENTER key
```

(4) After entering an Ethernet Address input, enter "ENTER" through the keyboard.

(5) If the contents of setting are checked and known to be correct, enter "2-ENTER" through the keyboard.

(6) Enter any key input.

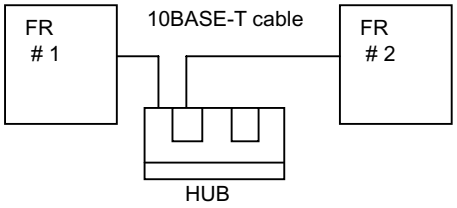
(7) Enter "0-ENTER" through the keyboard. (To the Inline Test Menu)

(8) Enter "0-ENTER" through the keyboard. (To the Main Menu)

(9) Enter "0-ENTER" through the keyboard. (Withdrawal from the diagnostic program)

15-2) Execution of Inline test

(1) Connect 2 FR units through the LAN cables via the hub.



FR # 1 : Machine under test
FR # 2 : Distant machine

(2) Enter "14-ENTER" through the keyboard for both FR#1 and FR#2.

LCD DISPLAY for FR#1 and FR#2

```
                  ***** TEST # 14 Inline Test. *****

                    0 : Return to MAIN MANU
                    1 : Set Configutation
                    2 : Send Data
                    3 : Receive Data
                    4 : Self Test


                  Select and press ENTER key : 0
```

(3) Send a key input of 3-ENTER to FR#2. R Data reception standby state

LCD DISPLAY for FR#2

```
                  ***** TEST # 14 Inline Test. *****


     ***** Receive Data *****
```

(4) Send a key input of 2-ENTER to FR#1.

LCD DISPLAY for FR#1

```
                  ***** TEST # 14 Inline Test. *****

     ***** Send Data *****

     Send Data            1234567890AB     >>>     FFFFFFFFFFFF     OK
```

(5) When data are received from FR#1, FR#2 then displays the following screen:

LCD DISPLAY for FR#2

```
                ***** TEST # 14 Inline Test. *****

    ***** Receive Data *****

    Receive Data          1234567890AB     >>>     FFFFFFFFFFFF     OK
    Send Data             ABCDEF123456     >>>     1234567890AB     OK

Test done. Press any key
```

(6) When data are received from FR#2, FR#1 then displays the following screen:

LCD DISPLAY

```
                ***** TEST # 14 Inline Test. *****

    ***** Receive Data *****

    Send Data             1234567890AB     >>>     FFFFFFFFFFFF     OK
    Receive Data          ABCDEF123456     >>>     1234567890AB     OK

Test done. Press any key
```

(7) Check the display of OK and finish the test.

(8) Confirm in the middle of testing that the front LED for LAN blinks in green.

(9) For both FR#1 and FR#2, press any key to obtain a test screen for #14. In addition, enter "0-ENTER" through the keyboard to obtain a menu screen for the diagnostic program.

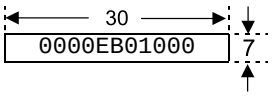
15-3) Registration of LAN system address

For each FR, individually register and control the ID address of the network (12-digit hexadecimal number).

Control numbers : Within the range of 0000EB010000 ~ 0000EB01FFFF (12-digit hexadecimal number)

Method of registration

(1) Write the above number on the label and stick it to the MAIN PWB.



Method of control

(1) Irrespective of the product item number, this label shall be stuck to the PWB where the LAN controller is mounted. Since this method is used for multiple models, control must be carefully done to avoid duplication or lack of numbering.

16) Mouse test

(1) Turn on the power supply under the condition that the keyboard and the mouse are connected to the keyboard connector through the mouse inspection branch cables.

(2) Enter a key input of 15-ENTER from the Main Menu.

LCD DISPLAY

```
                ***** TEST # 15 Mouse Test. ****

     Mouse Interface Test   Mouse Interface OK       _



   ENTER 1 (OK) or 2 (NG)

                                          1 (OK)  2 (NG)
```

(3) Confirm that "Mouse Interface OK" is displayed and enter an input of the "1" key.

LCD DISPLAY

```
                ***** TEST # 15 Mouse Test. ****

     Mouse Interface Test   Mouse Interface OK       OK


    Test done. Press any key.

                                                EXIT
```

(4) Press any key to recover the Main Menu.

(5) Disconnect the mouse from the connector. Enter a key input of 15-ENTER again from the Main Menu.

LCD DISPLAY

```
                ***** TEST # 15 Mouse Test. ****

     Mouse Interface Test   Mouse Interface ERROR    _



   ENTER 1 (OK) or 2 (NG)

                                          1 (OK)  2 (NG)
```

(7) Confirm that "Mouse Interface ERROR" is displayed and enter a key input of 1-ENTER.

LCD DISPLAY

```
                ***** TEST # 15 Mouse Test. ****

     Mouse Interface Test   Mouse Interface OK       OK



    Test done. Press any key.

                                                EXIT
```

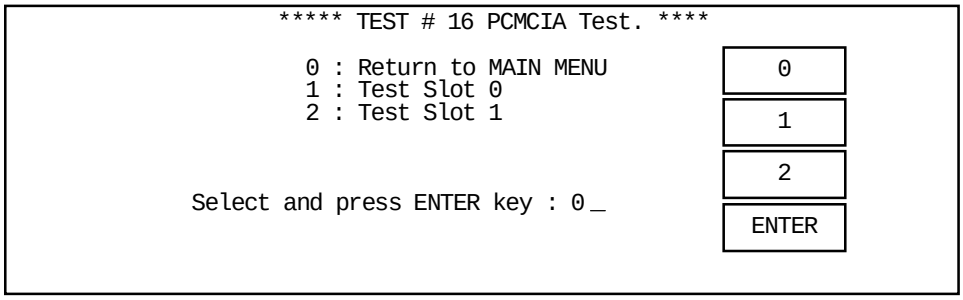
(8) Press any key to recover the Main Menu.

17) PCMCIA test (PCI slot test)

(1) Insert the PCMCIA card.

(2) Enter "16-ENTER" through the keyboard.

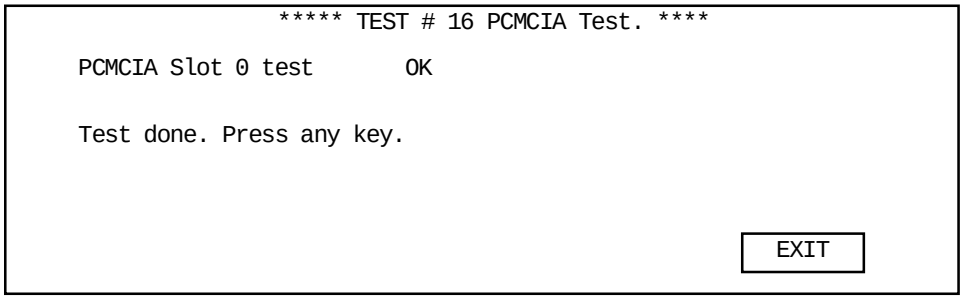
LCD DISPLAY



(3) Insert the PCMCIA card in Slot 0 (top).

(4) Enter "1-ENTER" through the keyboard.

LCD DISPLAY



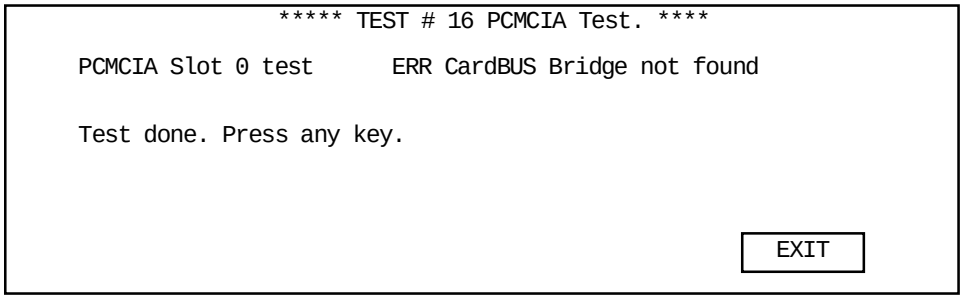
(5) Finish the test after displaying OK for the test result.

(6) Press any key to obtain the #16 Test screen.

(7) Remove the test card from Slot 0

(8) Enter "1-ENTER" through the keyboard.

LCD DISPLAY



(9) The test result shall result in "ERR CardBUS Beidge not found."

18) Flash Memory test

(1) Enter "17-ENTER" through the keyboard.

LCD DISPLAY

```
            ***** TEST # 17 Flash Memory Test. ****

    FFF80000-FFF9FFFF : PROG.SAVE
    FFF80000-FFF9FFFF : TEST DATA W/R  (55AA)  TEST DATA W/R  (AA55)
    FFF80000-FFF9FFFF : PROG.LOAD
    FFFA0000-FFFBFFFF : PROG.SAVE
    FFFA0000-FFFBFFFF : TEST DATA W/R  (55AA)  TEST DATA W/R  (AA55)
    FFFA0000-FFFBFFFF : PROG.LOAD
    FFFC0000-FFFDFFFF : PROG.SAVE
    FFFC0000-FFFDFFFF : TEST DATA W/R  (55AA)  TEST DATA W/R  (AA55)
    FFFC0000-FFFDFFFF : PROG.LOAD
    FFFE0000-FFFFFFFF : PROG.SAVE
    FFFE0000-FFFFFFFF : TEST DATA W/R  (55AA)  TEST DATA W/R  (AA55)
    FFFE0000-FFFFFFFF : PROG.LOAD
    Flash Memory OK
    Test done. Press any key.

                                                      EXIT
```

(2) The test result shall be OK.

(3) Press any key to obtain a menu screen for the diagnostic program.

19) USB test

(1) Enter "18-ENTER" through the keyboard.

LCD DISPLAY

```
                ***** TEST # 18 USB Test. ****

                 0 : Return to MAIN MENU
                 1 : USB Interface Test
                 2 : USB Keyboard Test

          Select and press ENTER key : 0_
```

0 | 1 | 2 | ENTER

(2) Set the USB low speed devices or the USB low speed jigs in both slots.

(3) Enter "1-ENTER" through the keyboard.

LCD DISPLAY

```
                ***** TEST # 18 USB Test. ****

USB Interface Test PORT 0       Low speed device connected
USB Interface Test PORT 1       Low speed device connected


ENTER 1 (OK) or 2 (NG)
```

1 (OK) | 2 (NG)

(4) Finish the test after displaying "Low speed device connected" for the test result.

(5) If the result is OK, press the "1" key. Otherwise, press the "2" key.

(6) Press any key to obtain a test screen of #19.

(7) Set the USB low speed devices or the USB low speed jigs in both slots.

(8) Enter "1-ENTER" through the keyboard.

LCD DISPLAY

```
                ***** TEST # 18 USB Test. ****

USB Interface Test PORT 0       High speed device connected
USB Interface Test PORT 1       High speed device connected


ENTER 1 (OK) or 2 (NG)
```

1 (OK) | 2 (NG)

(9) Finish the test after displaying "High speed device connected" for the test result.

(10) If the result is OK, press the "1" key. Otherwise, press the "2" key.

(11) Press any key to obtain a test screen of #19.

(12) Remove the USB jigs from both slots.

(13) Enter "1-ENTER" through the keyboard.

LCD DISPLAY

```
                    ***** TEST # 18 USB Test. ****

USB Interface Test PORT 0       USB device not connected
USB Interface Test PORT 1       USB device not connected


ENTER 1 (OK) or 2 (NG)


                                              1 (OK)   2 (NG)
```

(14) Finish the test after displaying "USB device not connected" for the test result.

(15) If the result is OK, press the "1" key. Otherwise, press the "2" key.

(16) Press any key to obtain a test screen of #19.

(17) Enter "0-ENTER" through the keyboard to obtain a menu screen for the diagnostic program.

20) HEAT RUN test

(1) Enter "19-ENTER" through the keyboard.

(2) For the 4 items specified below, carry out the heat run test for more than 10 hours.

(3) Enter a key input of F1 to stop the diagnostic services.

(4) Enter a key input of F2 to display the result of heat run test. Confirm that all the error items are "0" at that time.

LCD DISPLAY

```
        ***** TEST #19 Heat Run Test. *****    TEST COUNT  =**

                                 (ERROR TIMES)
Main Board Test.                       0
Random Access Memory Test.             0
Hard Disk Test.                        0
Video Test.                            0
Customer Display Test.                 0
Inline Test.                           0


F1=STOP/CONTINUE F2=STOP/MENU      TEST=RUN
```

(5) Enter a key input of F2 to obtain a menu screen for the diagnostic program.

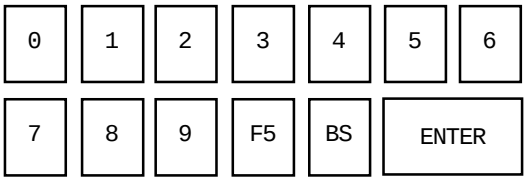
21) VGA Monitor Display test

(1) Connect a VGA monitor to the VGA connector.

(2) Turn on the FCR power supply and confirm that the screen as shown below is displayed.

LCD DISPLAY

```
                PANASONIC  JS-170FR TEST  PROGRAM V5.X

   0 : EXIT                              11 : Touch Panel Test.
*  1 : Main Board Test.                  12 : Magnetic Card Reader Test.
*  2 : Random Access Memory Test.        13 : Drawer Test.
   3 : Keyboard Test.                 *  14 : Inline Test.
   4 : Floppy Disk Test.                 15 : Mouse Test.
*  5 : Hard Disk Test.                   16 : PCMCIA Test.
*  6 : Video Test.                       17 : Flash Memory Test.
   7 : Parallel Port Test.               18 : USB Test.
   8 : Serial Port Test.                 19 : Heat Run Test.
   9 : Speaker Test.                     20 : Remote Test.
* 10 : Customer Display Test.
                Select and Press ENTER Key  :  0_
```

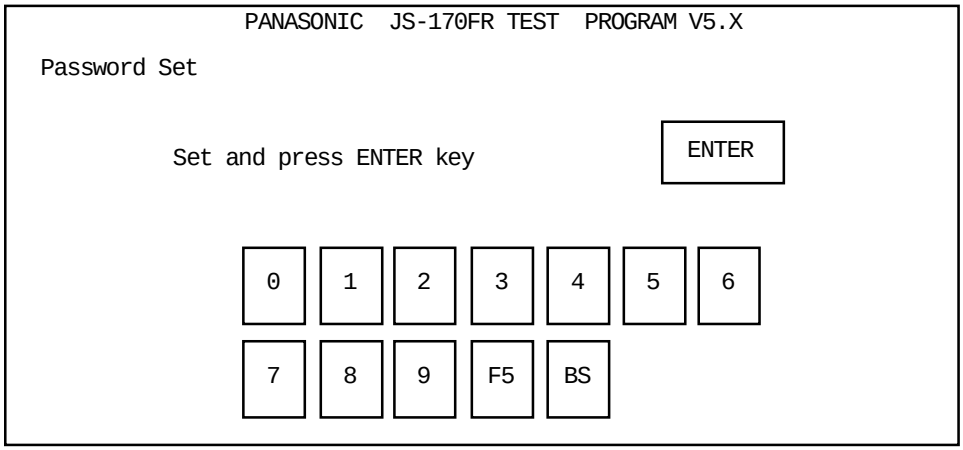


22) Input Password

The drawer test is locked by the password. Execute this test to unlock it.

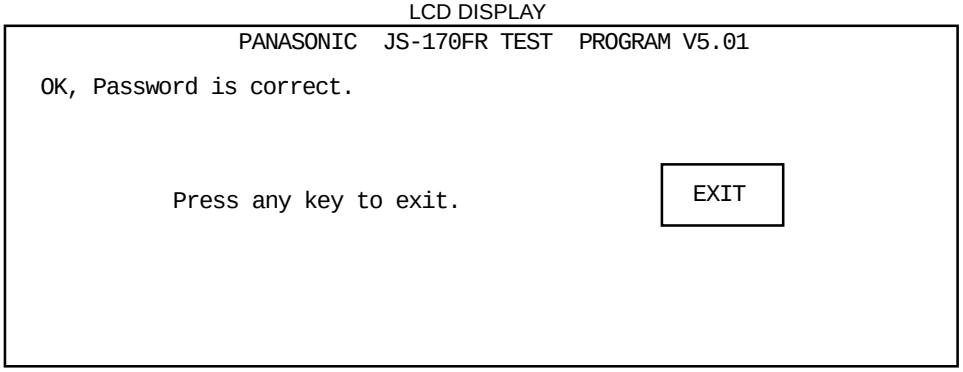
(1) Select 19 and press the [ENTER] key on the main menu.

LCD DISPLAY



(2) Enter 0427 on the keyboard or touch panel.

LCD DISPLAY



(3) When the screen appears as shown above, press any key to return to the main menu.
(If you have failed, try again from Step (1).)

23) Operation Checks after Diagnostic Services

When all test programs have been over, arrange the HDD and the BIOS under the shipping condition.

(1) Finish the diagnostic programs and display the DOS prompt.

```
c:>
```

(2) After entering the chpos input, press the Enter key.

```
c:>chpos
```

When c:> is displayed, turn off the FCR power supply.

(3) Turn on the power supply for the JS-170FR and confirm that the screen as shown below is displayed.

```
Staring MS-DOS
HIMEM is testing extended memory...done.
C:\>C\DOS\SMARTRV.EXE\X
C:\>
```

(4) Dip SW1 on the main PCB factory setting

JS-170FR-U, C, EF, S, A, W

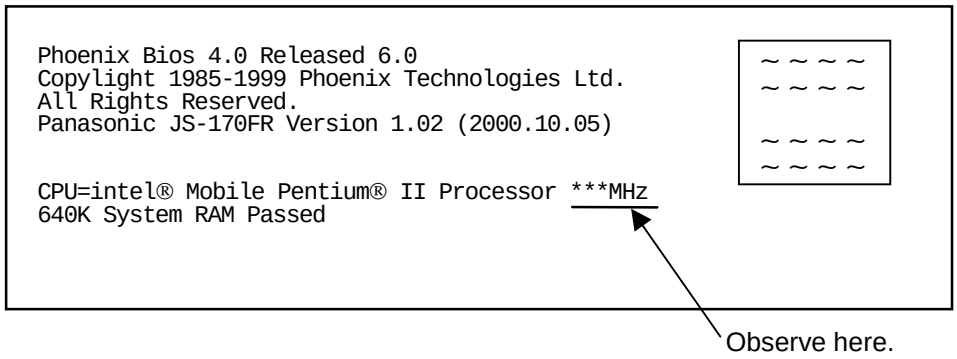
1	2	3	4	5	6
OFF	OFF	ON	ON	ON	ON

JS-170FR-G2*

1	2	3	4	5	6
OFF	ON	ON	ON	ON	ON

(5) Confirmation of the CPU operating frequency

Observe the product No. and CPU operating frequency on the following startup screen.


Phoenix Bios 4.0 Released 6.0
Copylight 1985-1999 Phoenix Technologies Ltd.
All Rights Reserved.
Panasonic JS-170FR Version 1.02 (2000.10.05)
CPU=intel® Mobile Pentium® II Processor ***MHz
640K System RAM Passed
Observe here.

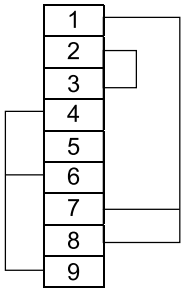
Product No.	Frequency
JS-170FR-*20, *21, *22, *23	266MHz
JS-170FR-*24, *25	333MHz

*: A, E, F, G, S, U, C, W

3.9 Materials for Reference

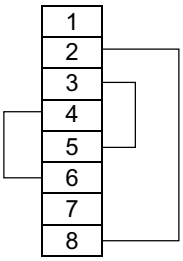
1) COM1, COM2 (RS-232C) loopback connectors

9-pin D-SUB (female)

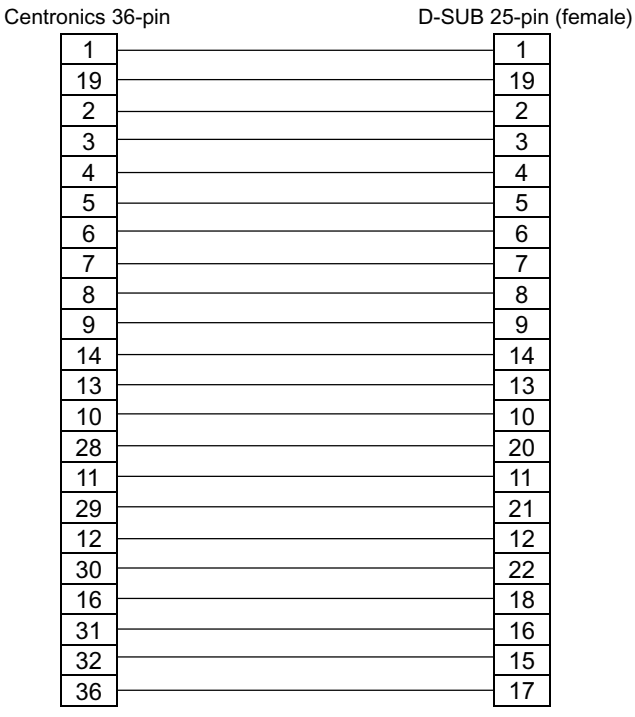


2) COM3 (RS-232C) loopback connector

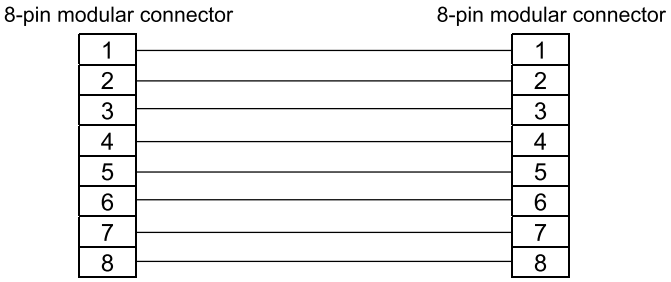
8-pin modular connector



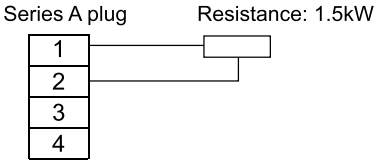
3) Printer cable connection diagram



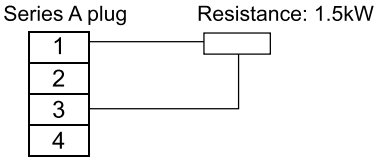
4) LAN interface cable



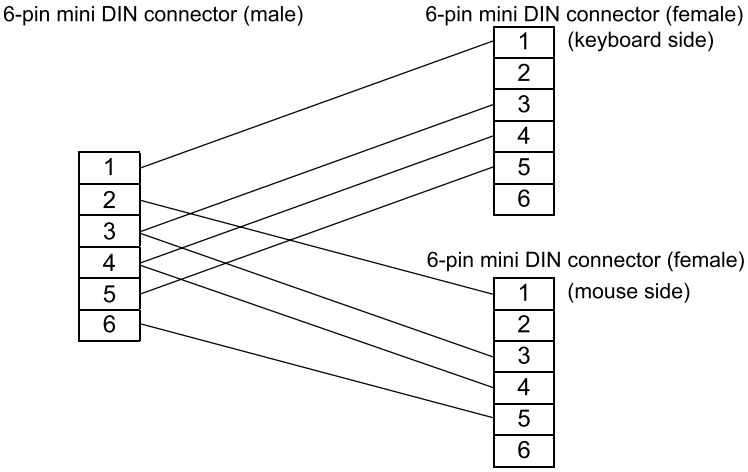
5) USB low speed jig



6) USB high speed jig



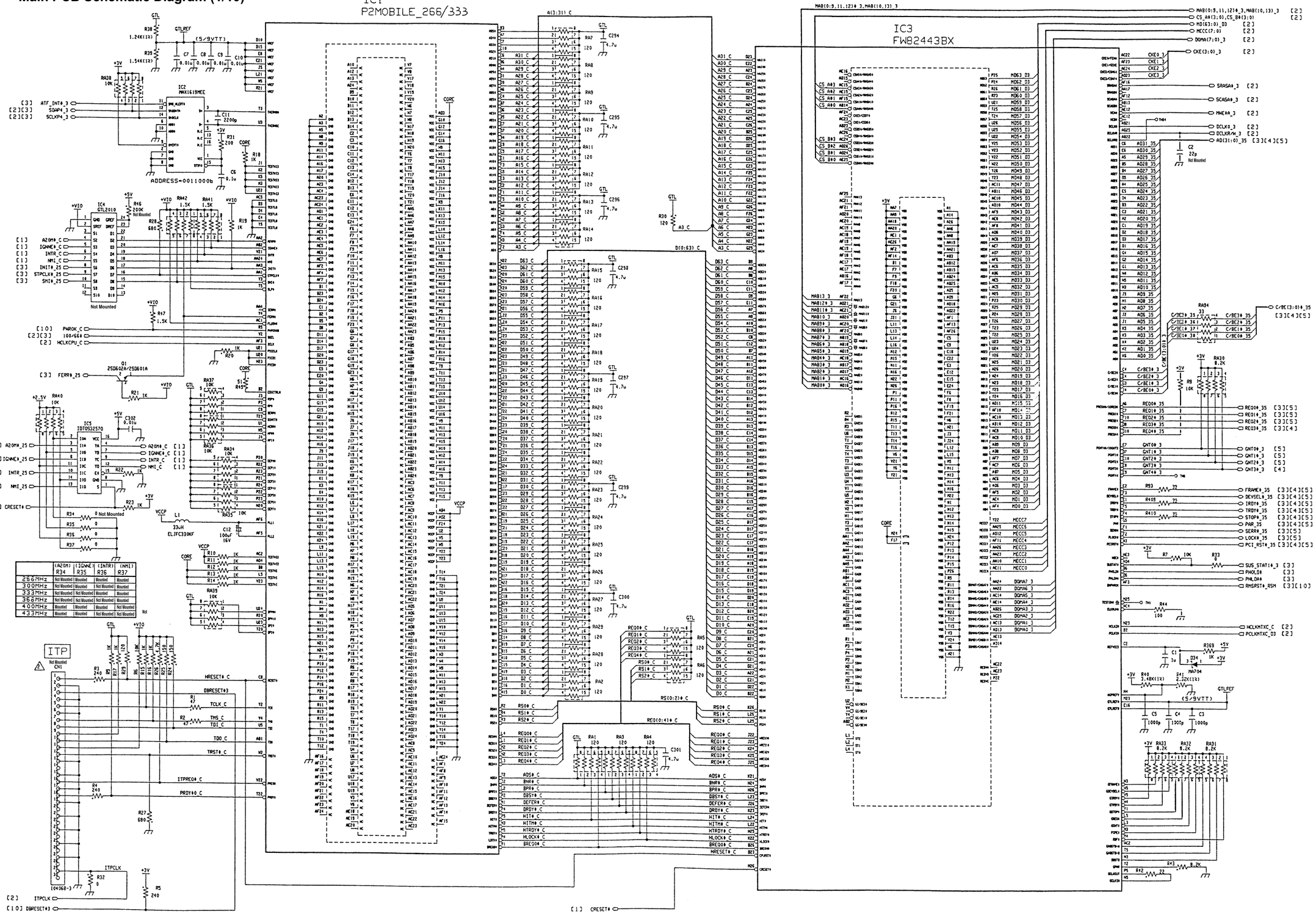
7) Mouse testing jig



4 JS-170FR-** PCB's

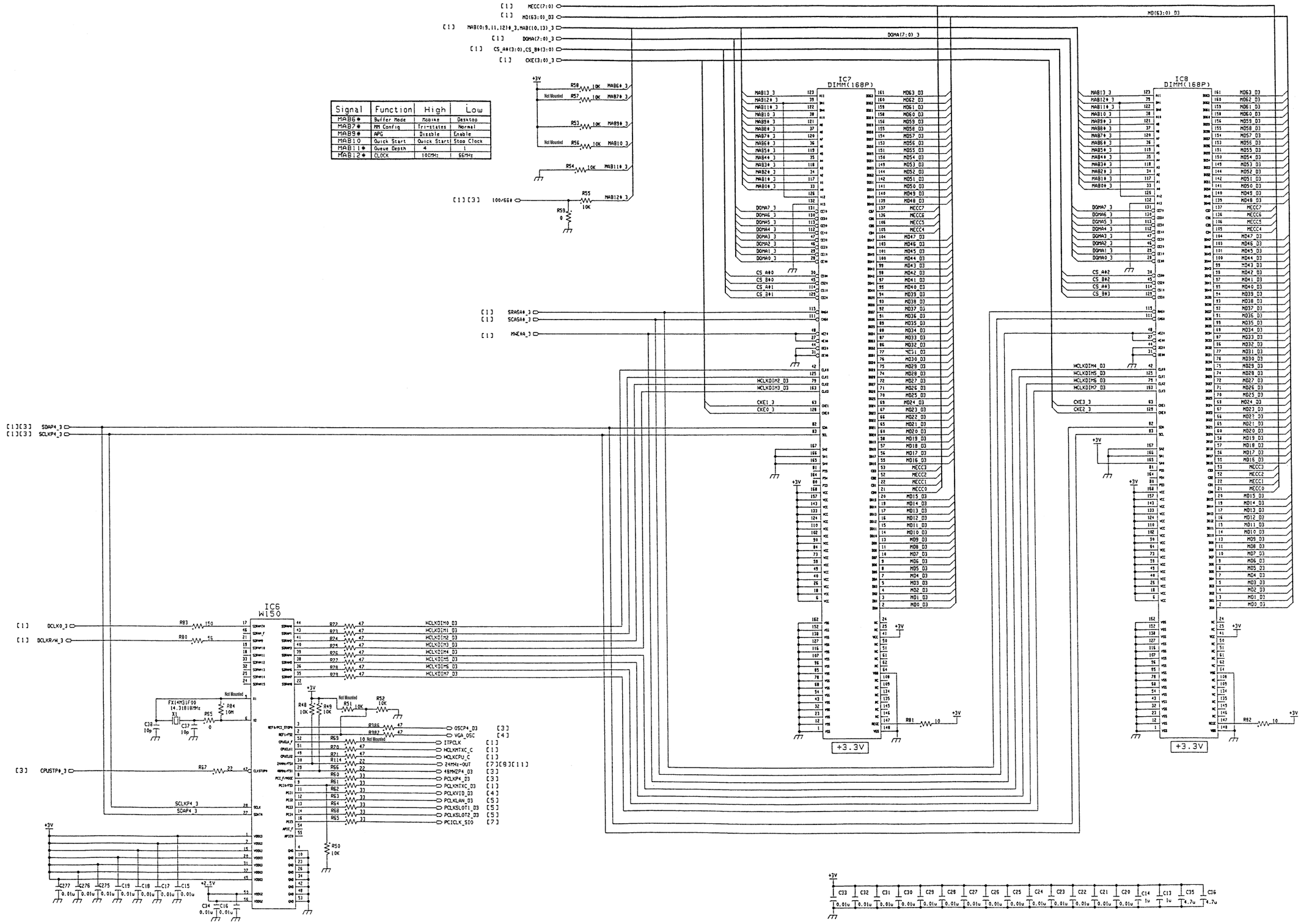
4.1 Main PCB

4.1.1 Main PCB Schematic Diagram (1/10)



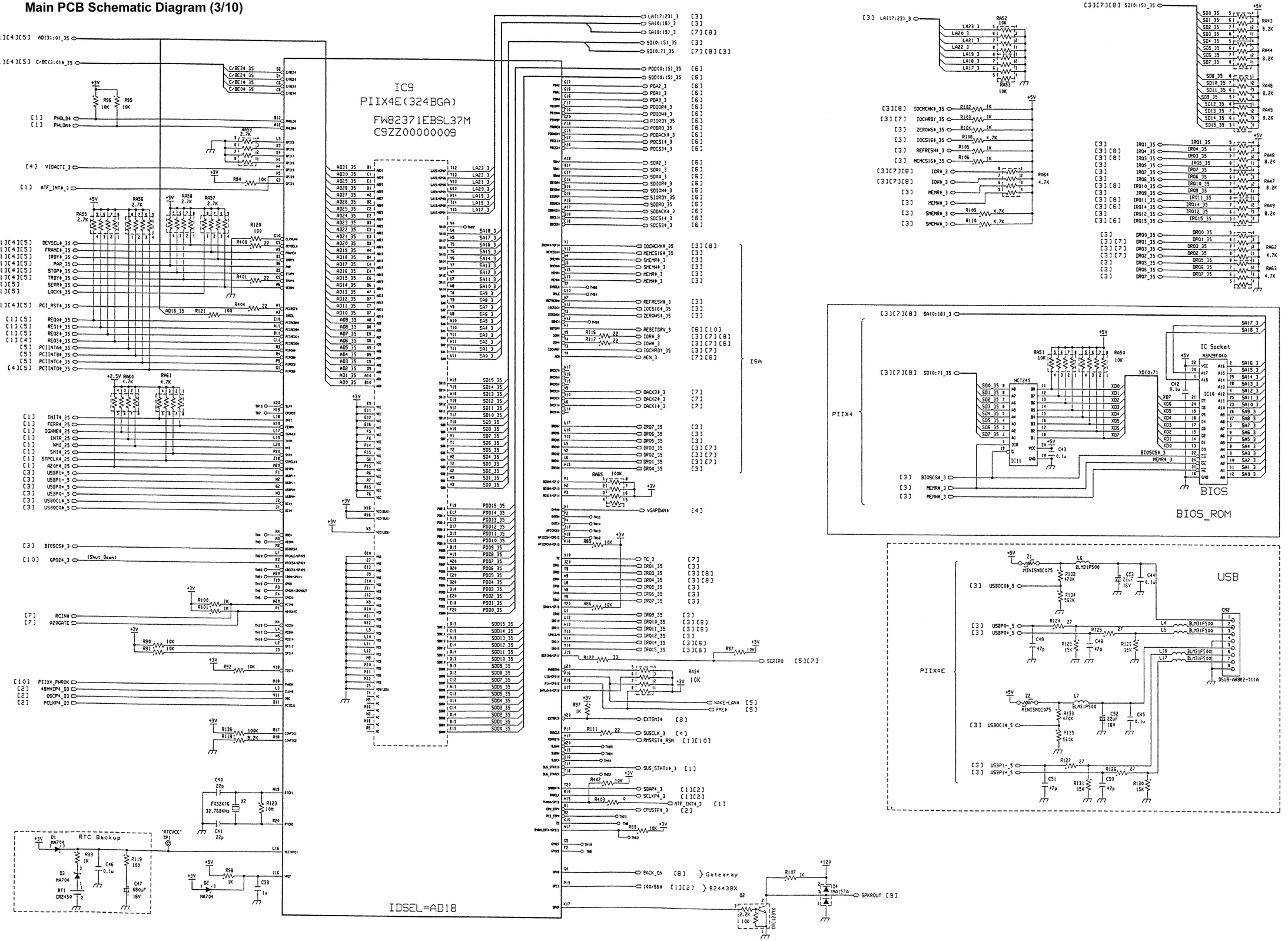
	(A20M) R34	(IGNNE) R35	(INTR) R36	(NMI) R37
266MHz	Not Mounted	Mounted	Mounted	Mounted
300MHz	Not Mounted	Mounted	Not Mounted	Mounted
333MHz	Not Mounted	Not Mounted	Mounted	Mounted
366MHz	Not Mounted	Not Mounted	Not Mounted	Mounted
400MHz	Mounted	Mounted	Mounted	Not Mounted
433MHz	Mounted	Mounted	Not Mounted	Not Mounted

4.1.1 Main PCB Schematic Diagram (2/10)

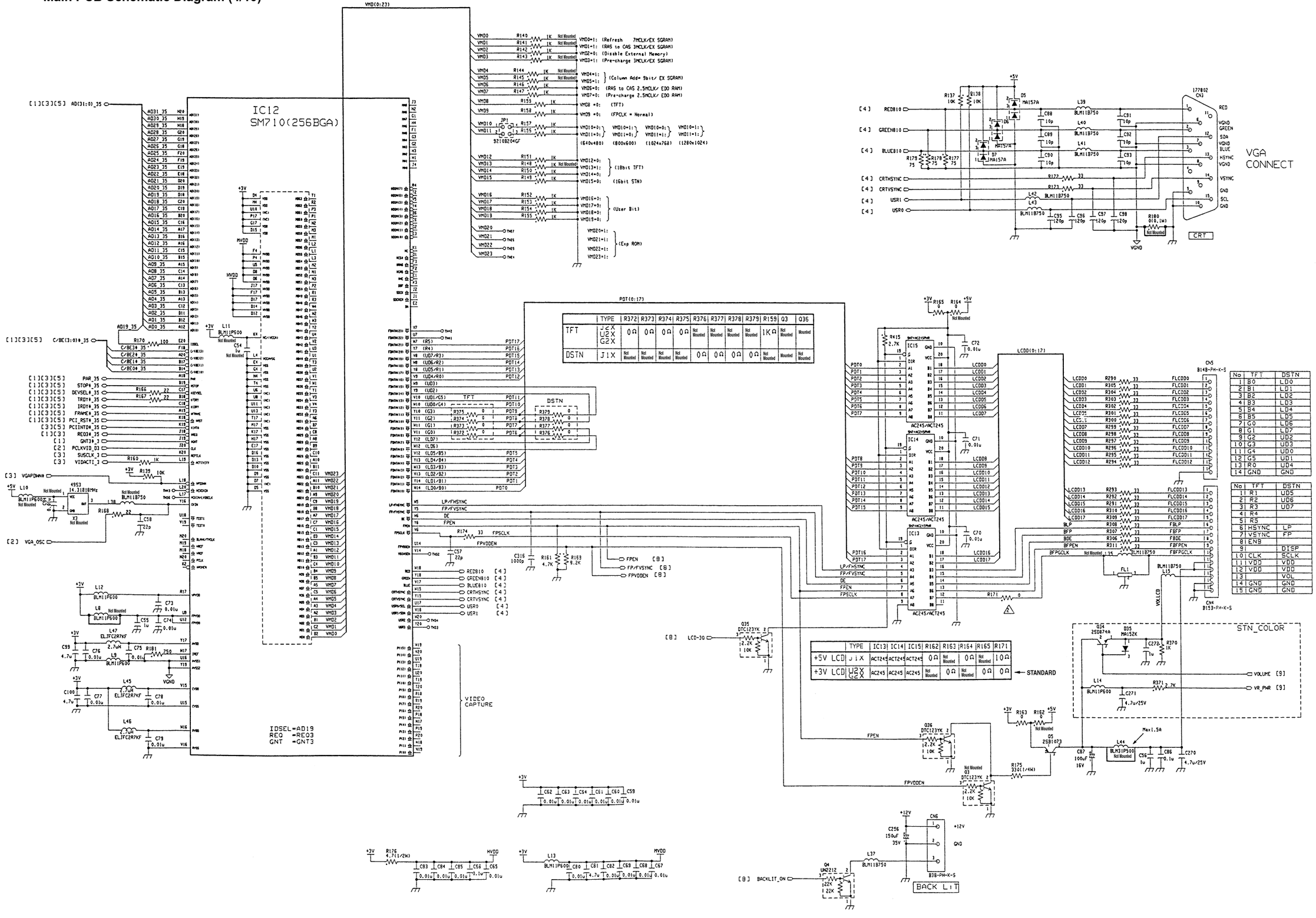


Signal	Function	High	Low
MAB6#	Buffer Mode	Mobile	Desktop
MAB7#	MM Config	Tri-states	Normal
MAB9#	APG	Disable	Enable
MAB10	Quick Start	Quick Start	Stop Clock
MAB11#	Queue Depth	4	1
MAB12#	CLOCK	100MHz	66MHz

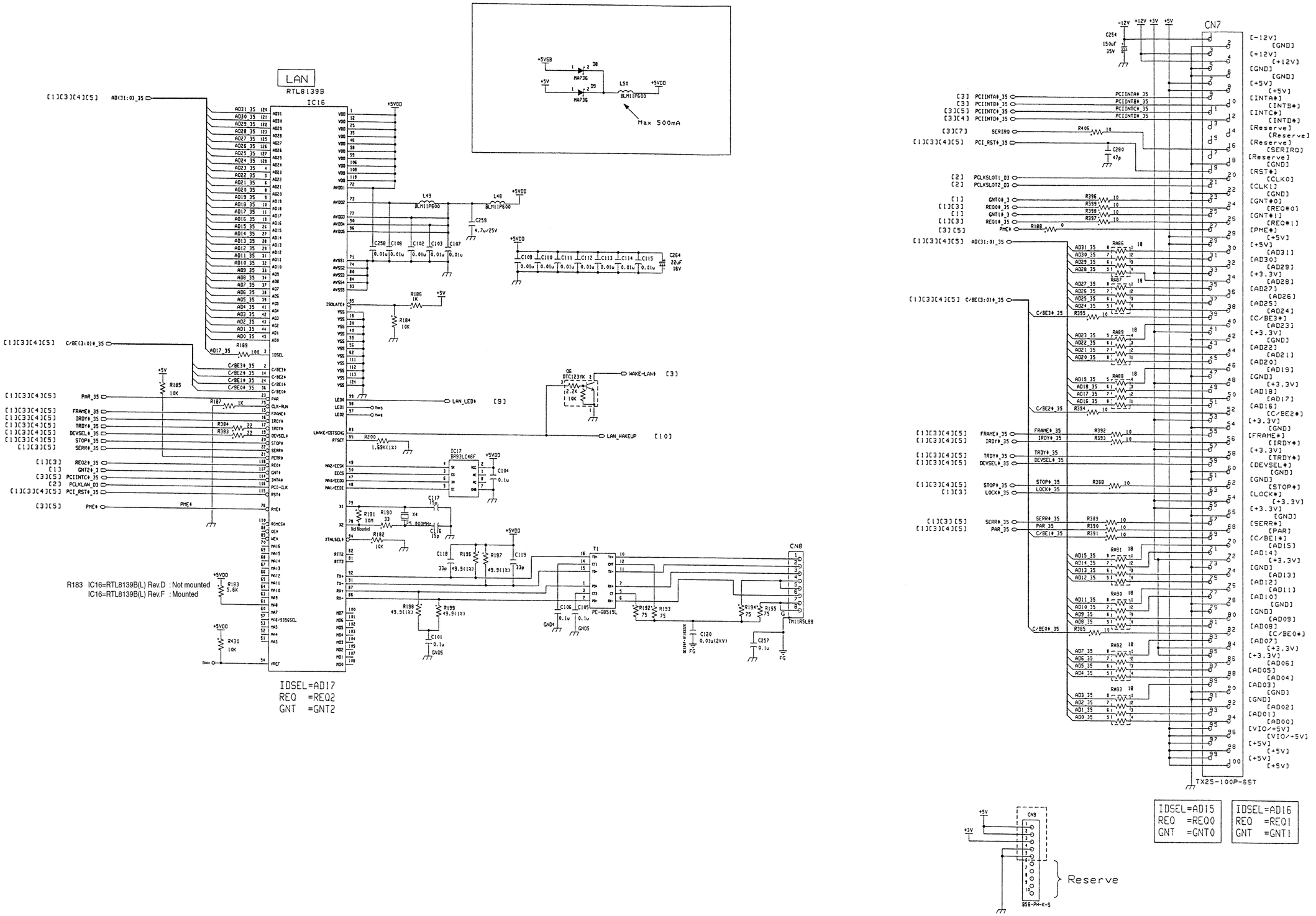
4.1.1 Main PCB Schematic Diagram (3/10)



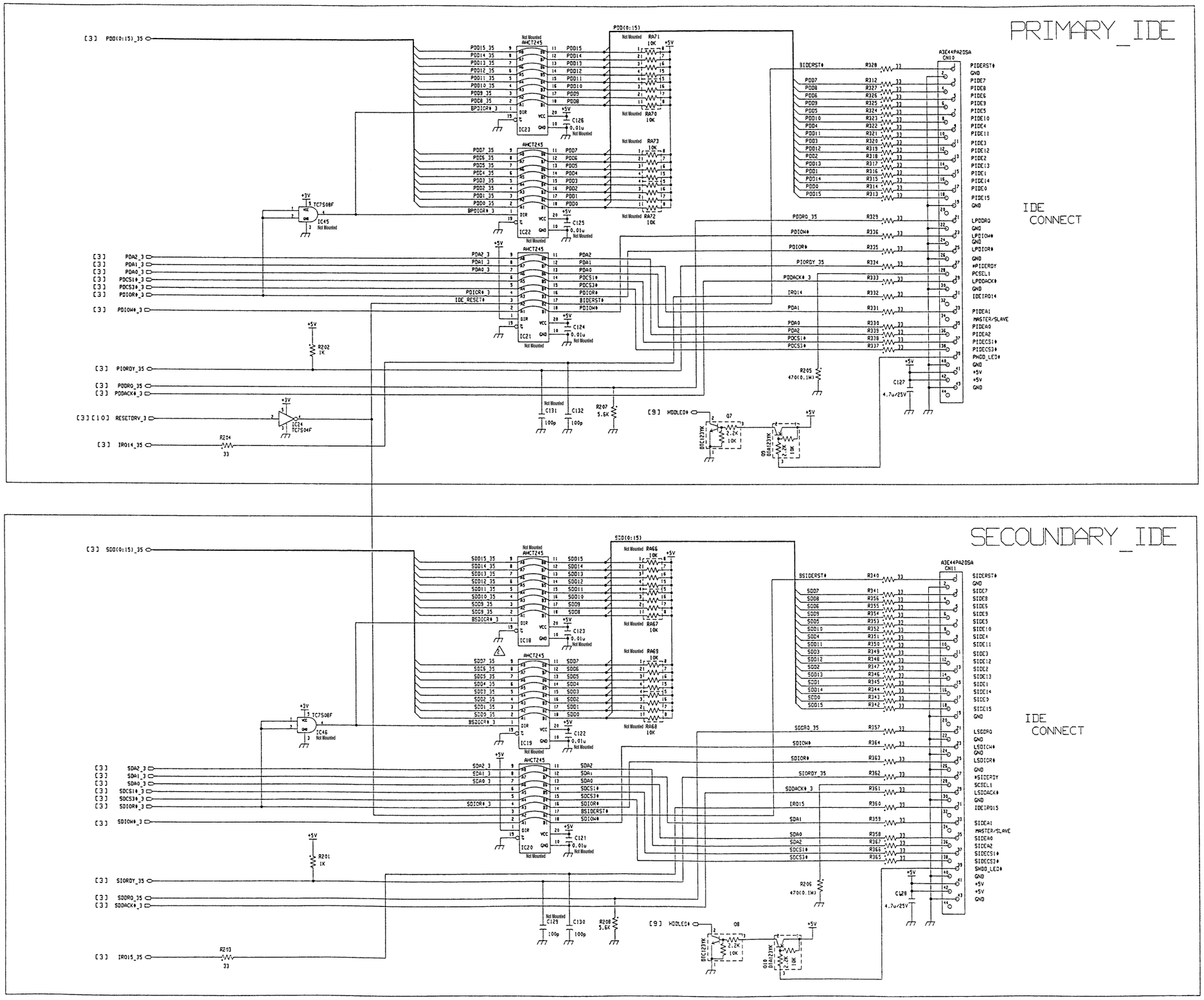
4.1.1 Main PCB Schematic Diagram (4/10)



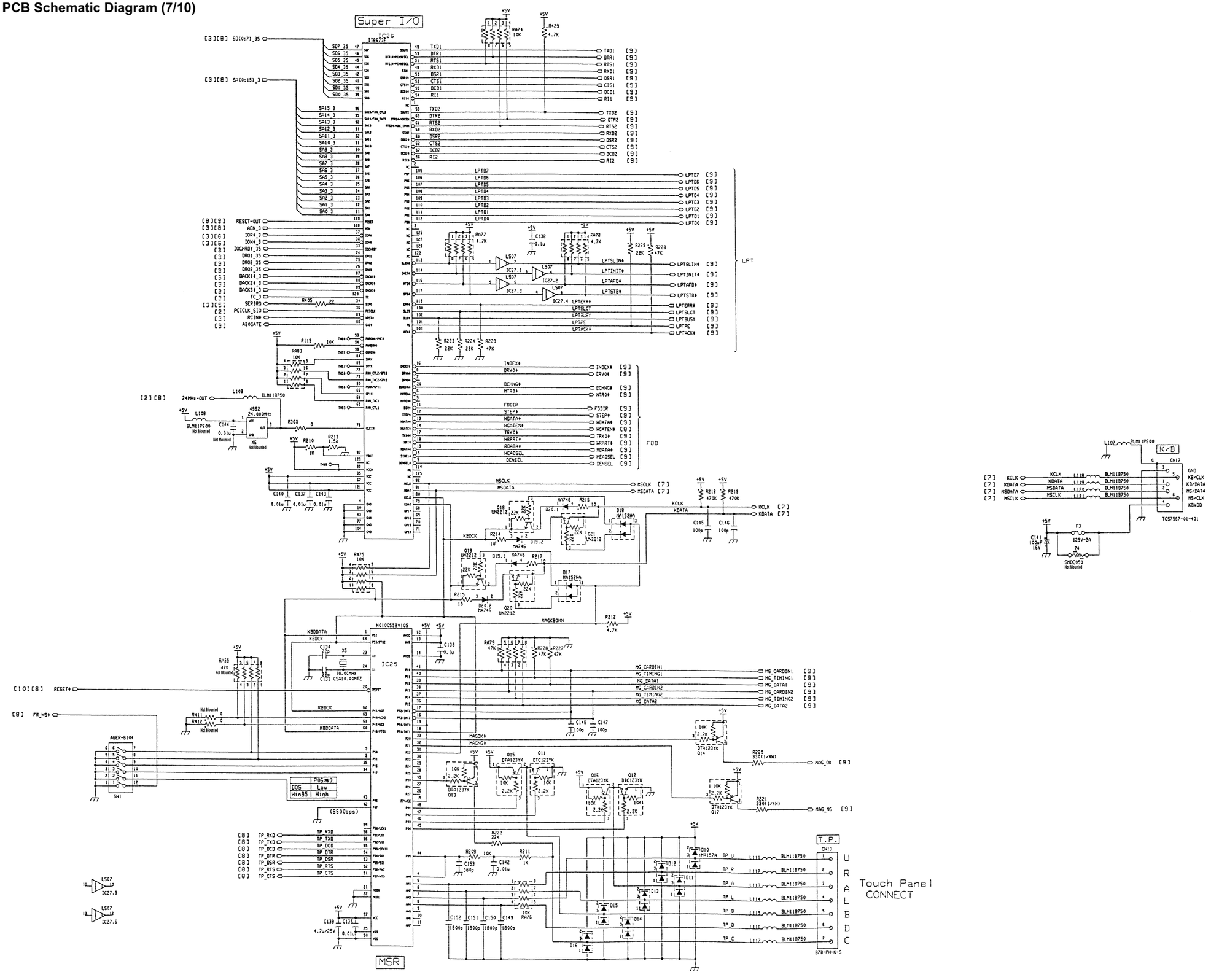
4.1.1 Main PCB Schematic Diagram (5/10)



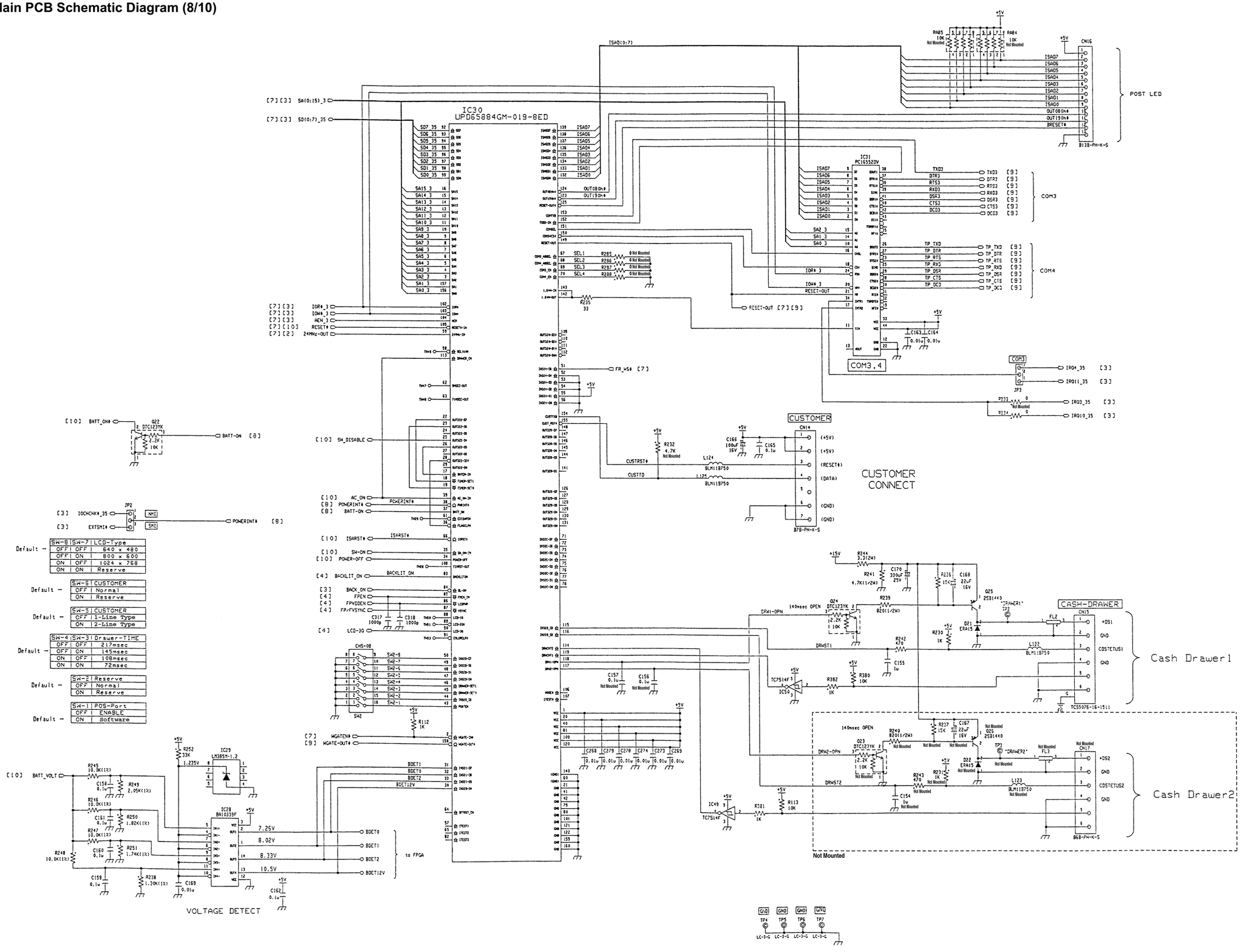
4.1.1 Main PCB Schematic Diagram (6/10)



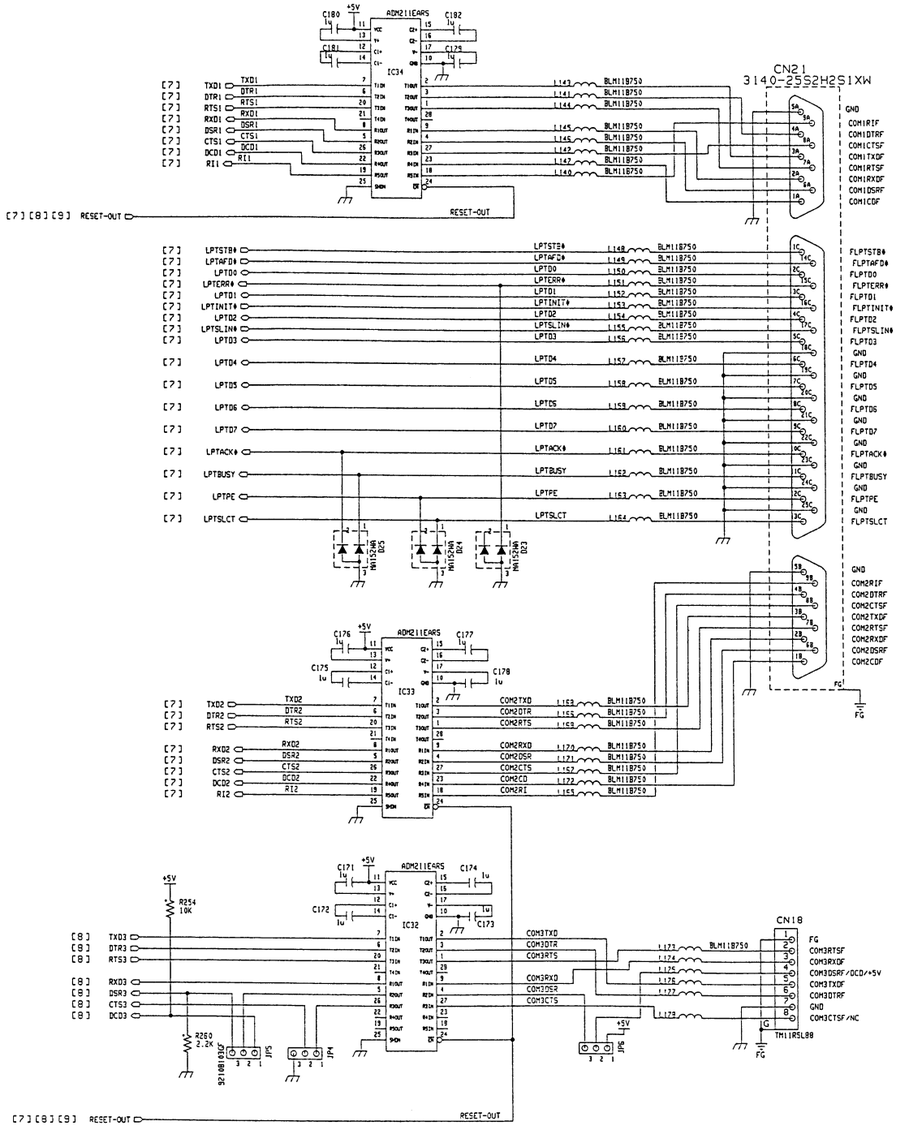
4.1.1 Main PCB Schematic Diagram (7/10)

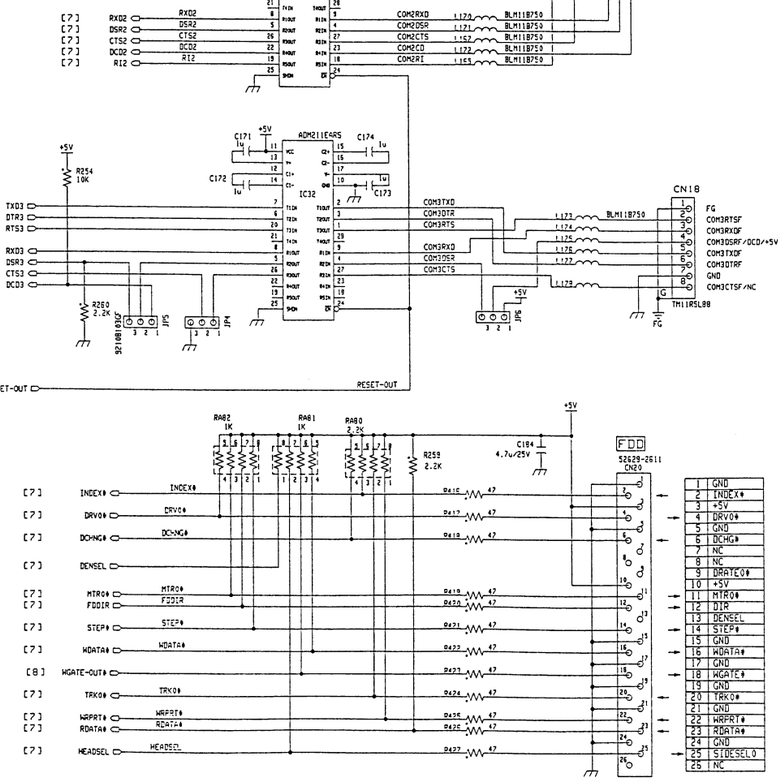


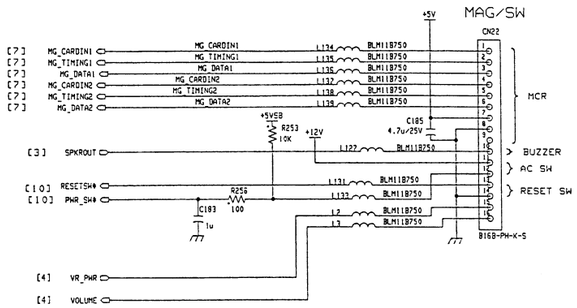
4.1.1 Main PCB Schematic Diagram (8/10)

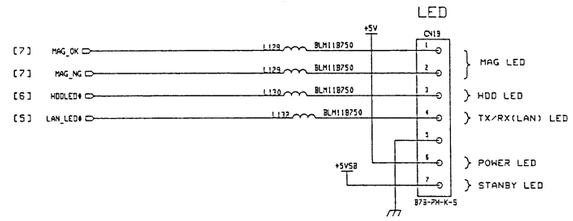


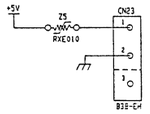
4.1.1 Main PCB Schematic Diagram (9/10)



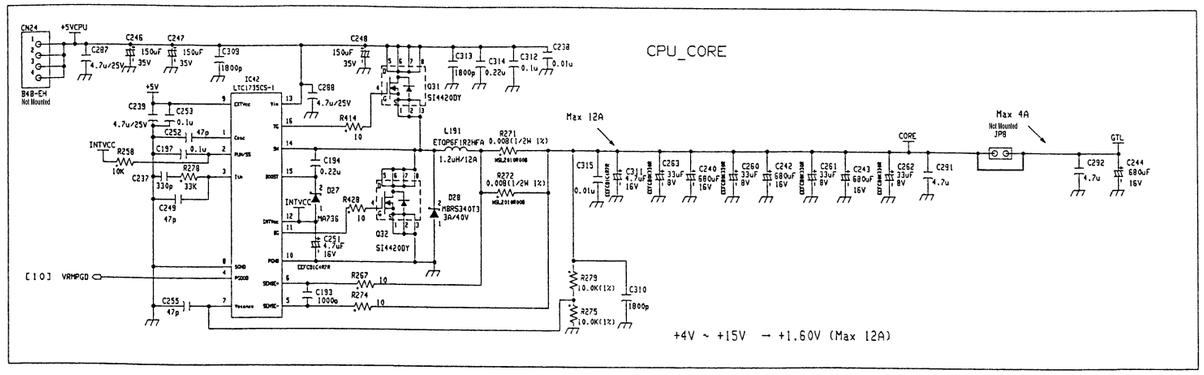


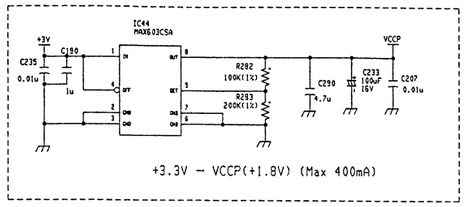


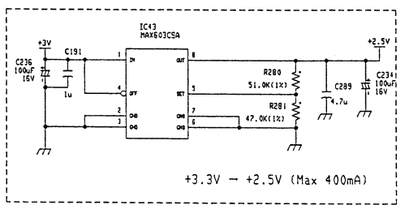


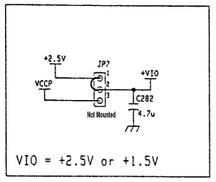


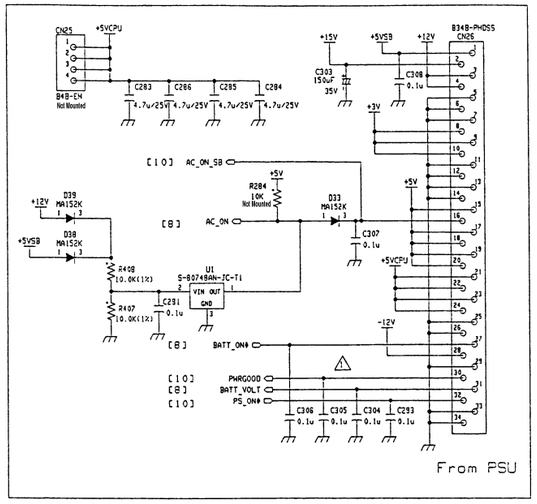
4.1.1 Main PCB Schematic Diagram (10/10)

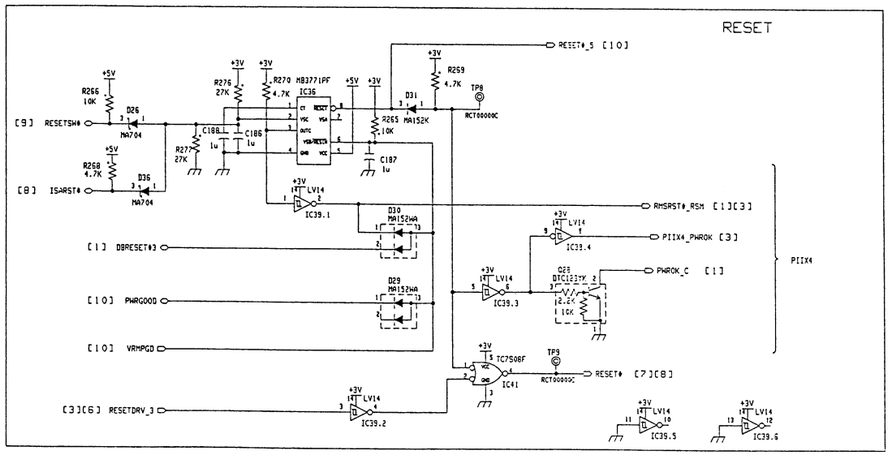


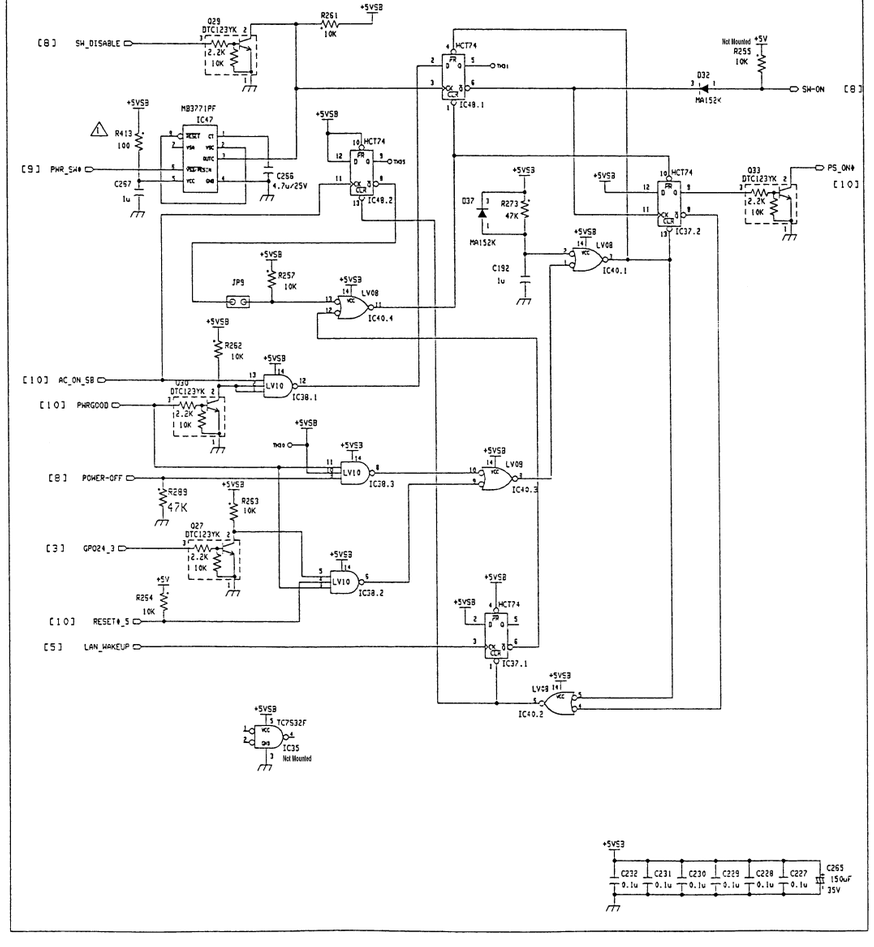


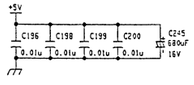


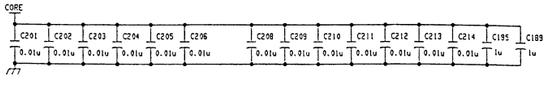


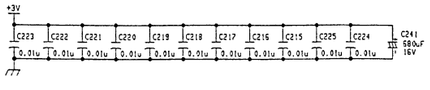




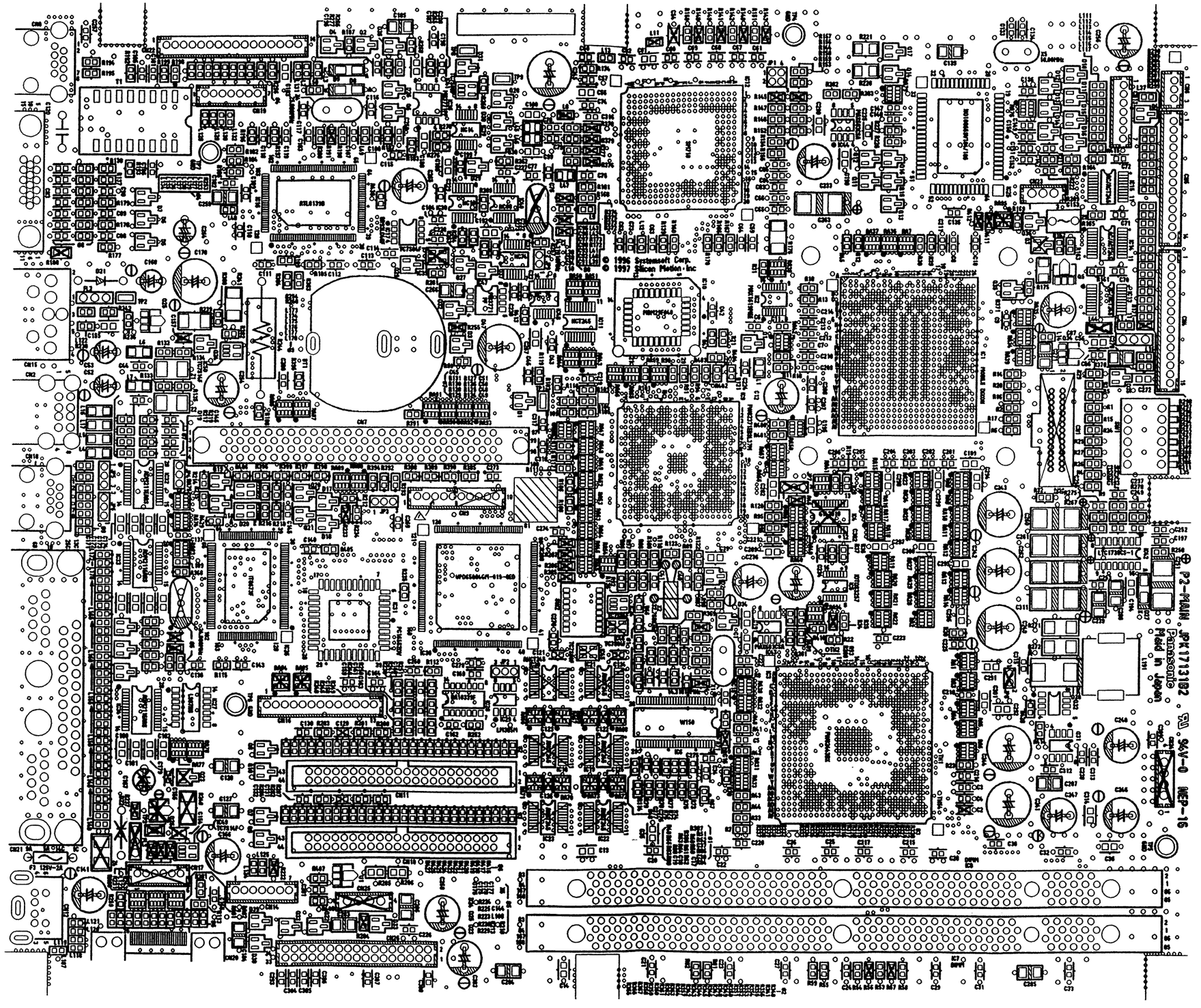






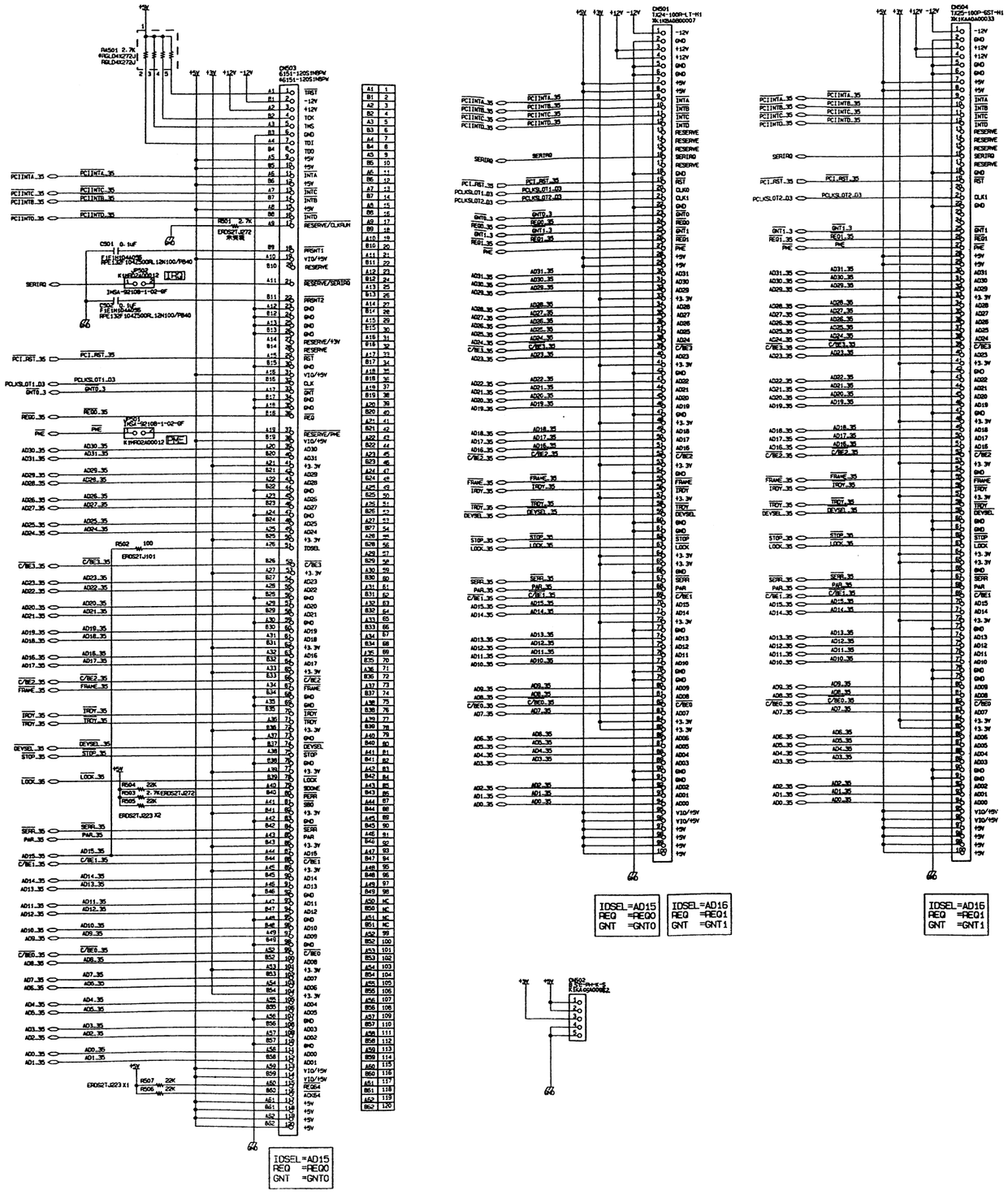


4.1.2 Main PCB Parts Location

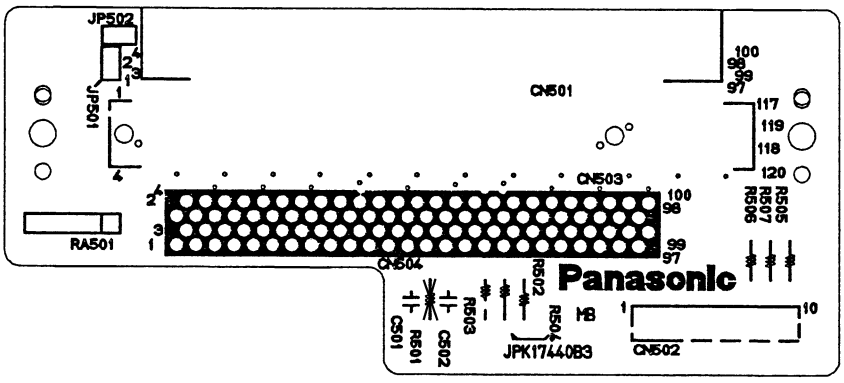


4.2 MB PCB

4.2.1 MB PCB Schematic Diagram



4.2.2 MB PCB Parts Location



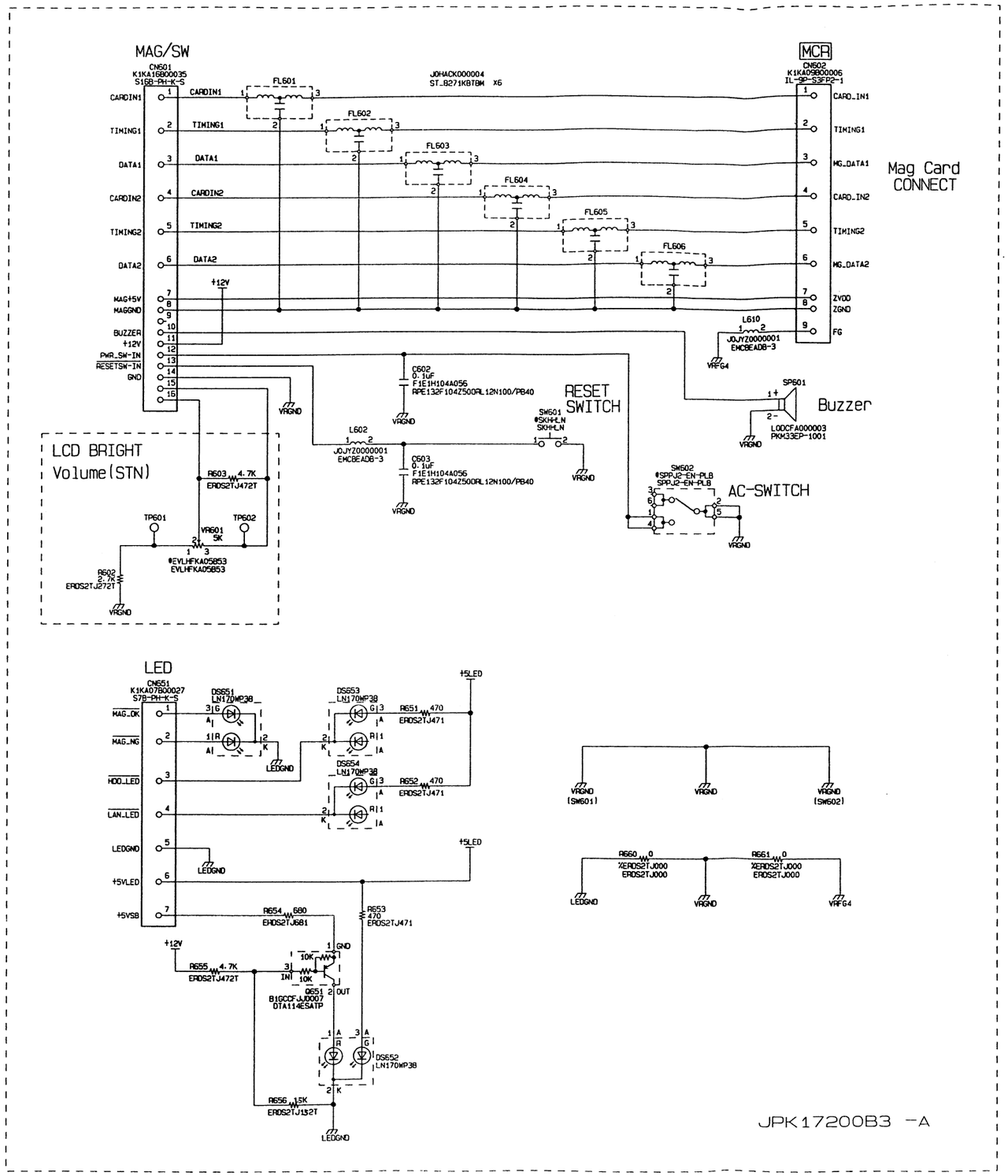
4.2.3 MB PCB Replacement Parts List

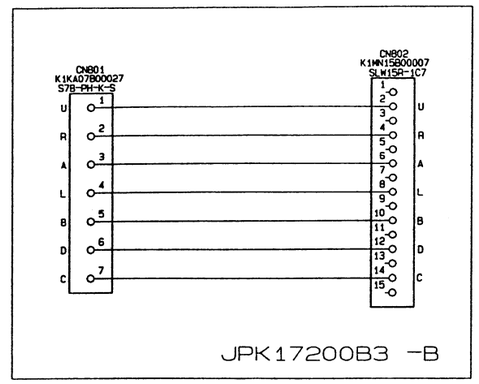
Note: When ordering replacement parts, indecate Part No. and Name of Parts.
RTL mark in Remarks means “Repairable PCB Assembly” “Retention Time Limited”.

Ref. No.		Part No.	Part Name & Description	Ps/set	Remarks
⑨⑨		P7FRJ20P3H	MB PCB	1	RTL
R 502		ERDS2TJ101	CARBON FILM RESISTOR	1	
R 503		ERDS2TJ272T	CARBON FILM RESESTOR	1	
R 504-507		ERDS2TJ223	CARBON FILM RESISTOR	4	
RA 501		D1ZZ00000021	RESISTOR-RESISTOR	1	
C 501-502		R32F104ZF01	CERAMIC CAPACITOR	2	
CN 501		K1KBA0B00007	CONNECTOR	1	
CN 502		YJB5B-PH-K-S	CONNECTOR	1	
CN 503		K1KBC0A00017	CONNECTOR	1	
CN 504		K1KAA0A00039	CONNECTOR	1	
		IMSA9215HGF	SOCKET	2	
P 501-502		YJ9210B102GF	PLUG	2	
		YJJDK23900B4	CABLE	1	

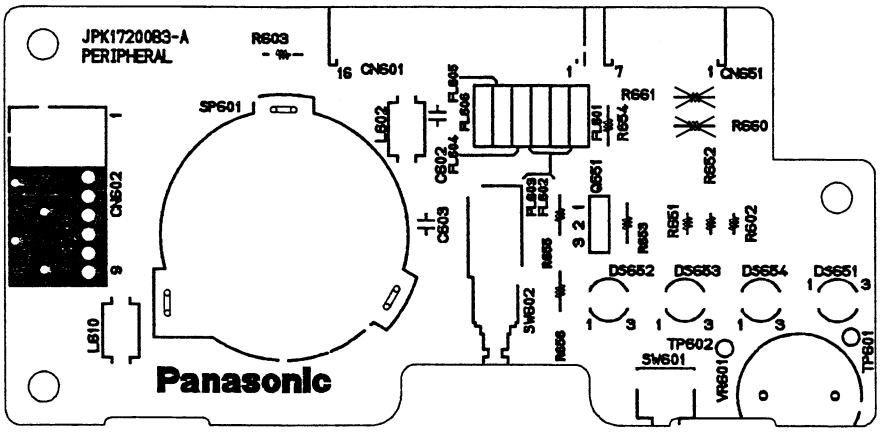
4.3 Peripheral PCB

4.3.1 Peripheral PCB Schematic Diagram





4.3.2 Peripheral PCB Parts Location



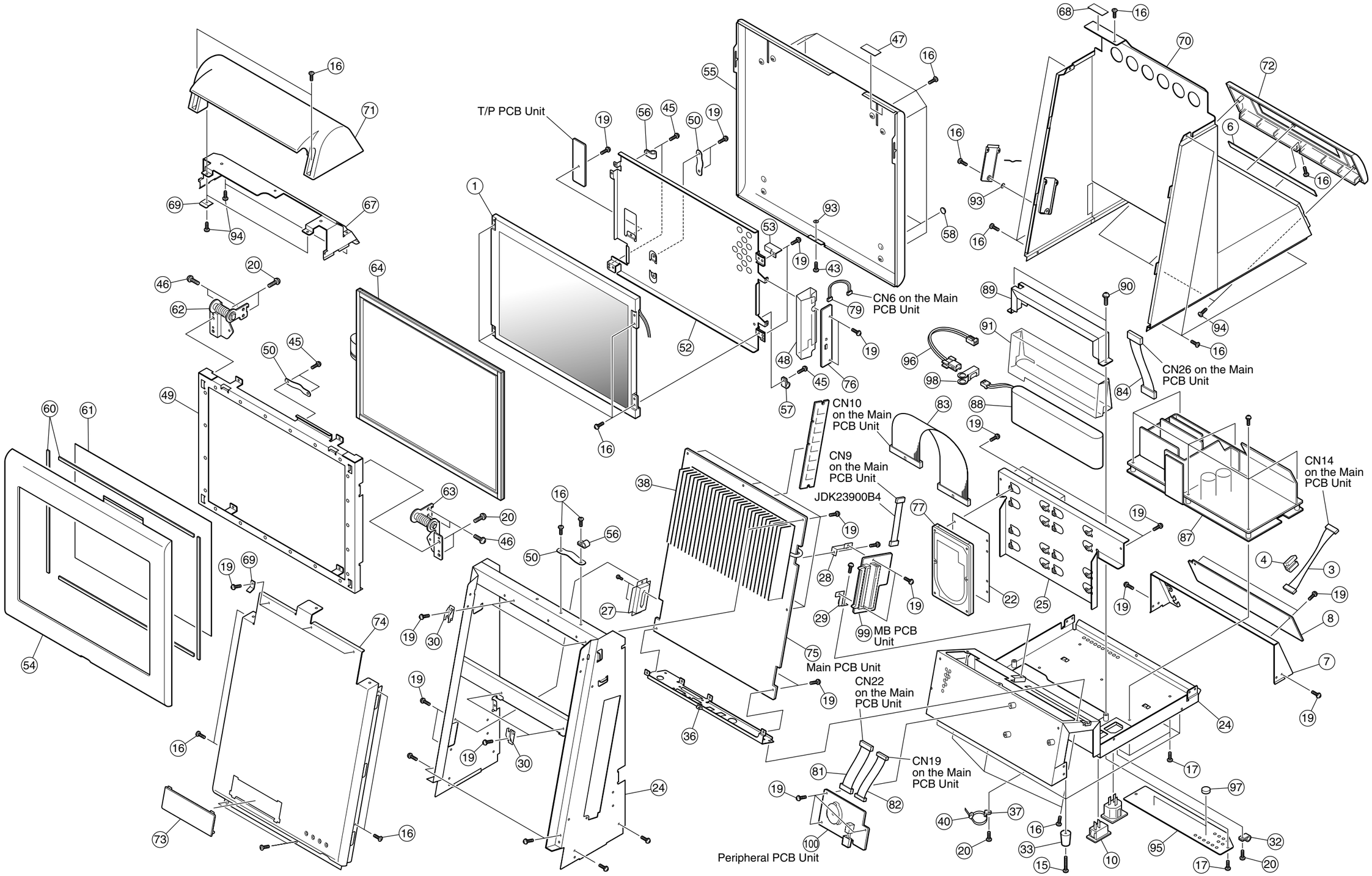
4.3.3 Peripheral PCB Replacement Parts List

Note: When ordering replacement parts, indecate Part No. and Name of Parts.
RTL mark in Remarks means “Repairable PCB Assembly” “Retention Time Limited”.

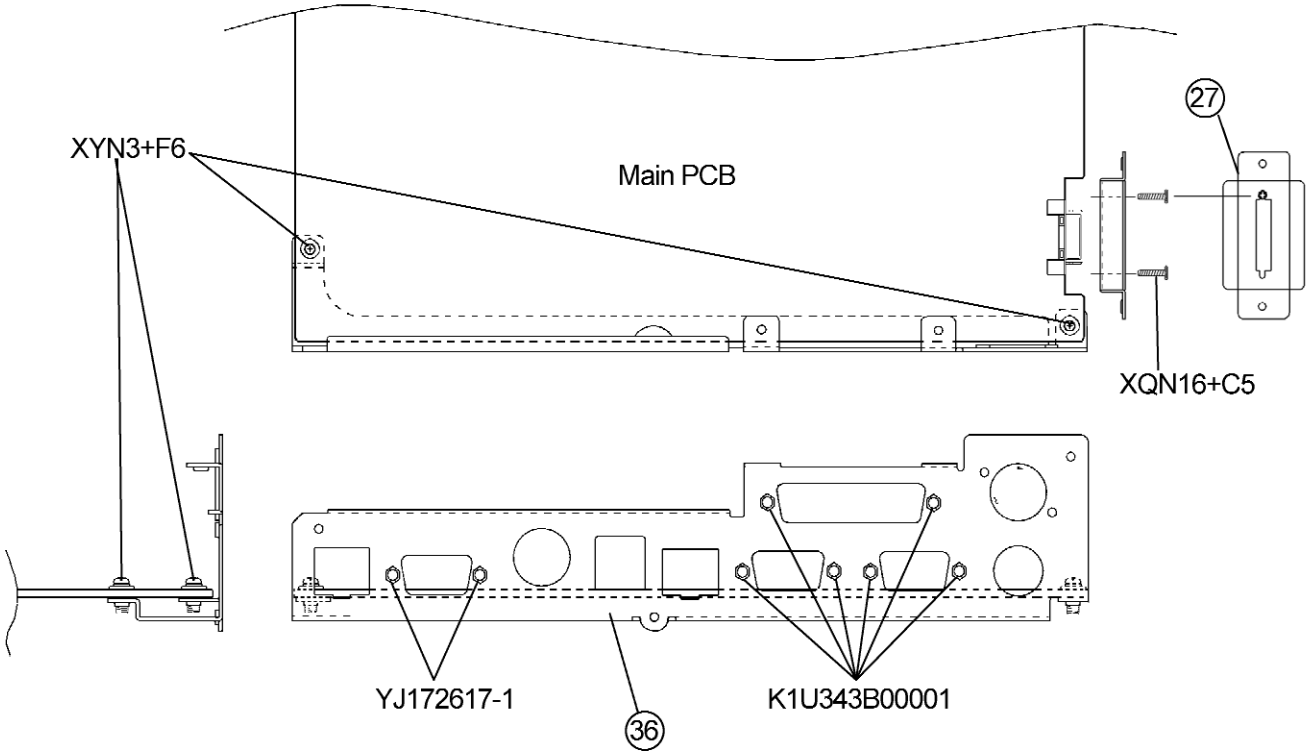
Ref. No.		Part No.	Part Name & Description	Ps/set	Remarks
(100)		P7FRJ20P2H	PERIPHERAL PCB	1	RTL
Q 651		DTA114ESATP	TRANSISTOR	1	
DS 651-654		LN170WP38	LED	4	
R 651-653		ERDS2TJ471	CARBON FILM RESISTOR	3	
R 654		ERDS2TJ681	CARBON FILM RESISTOR	1	
R 655		ERDS2TJ472T	CARBON FILM RESESTOR	1	
R 656		ERDS2TJ152T	CARBON FILM RESESTOR	1	
C 602-603		R32F104ZF01	CERAMIC CAPACITOR	2	
L 602.610		YJJNC00010B4	CHOKE COIL	2	
FL 601-606		YJSTB271KBTB	FILTER (DELAY LINE)	6	
BZ 601		PKM33EP-1001	BUZZER	1	
CN 601		S16B-PH-K-S	CONNECTOR	1	
CN 602		IL-9PS3FP2-1	CONNECTOR	1	
CN 651.801		YJS7B-PH-K-S	CONNECTOR	2	
CN 802		YJSLW15R-1C7	CONNECTOR	1	
SW 601		K0H1BB000039	PUSH SWITCH	1	
SW 602		K0F122B00077	PUSH SWITCH	1	
		K0YA00000015	PUSH SWITCH	1	

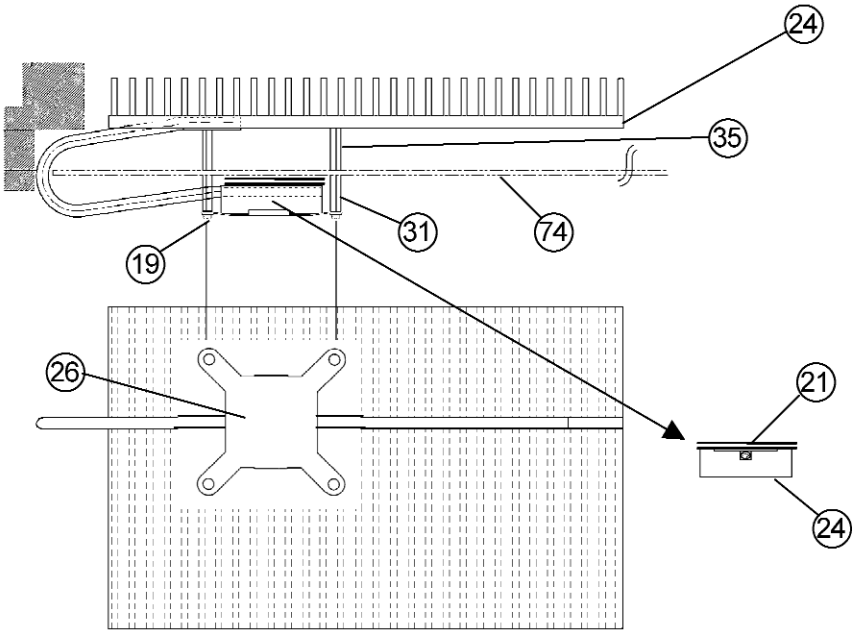
5 Body Block

5.1 Body Block Disassembling Drawing

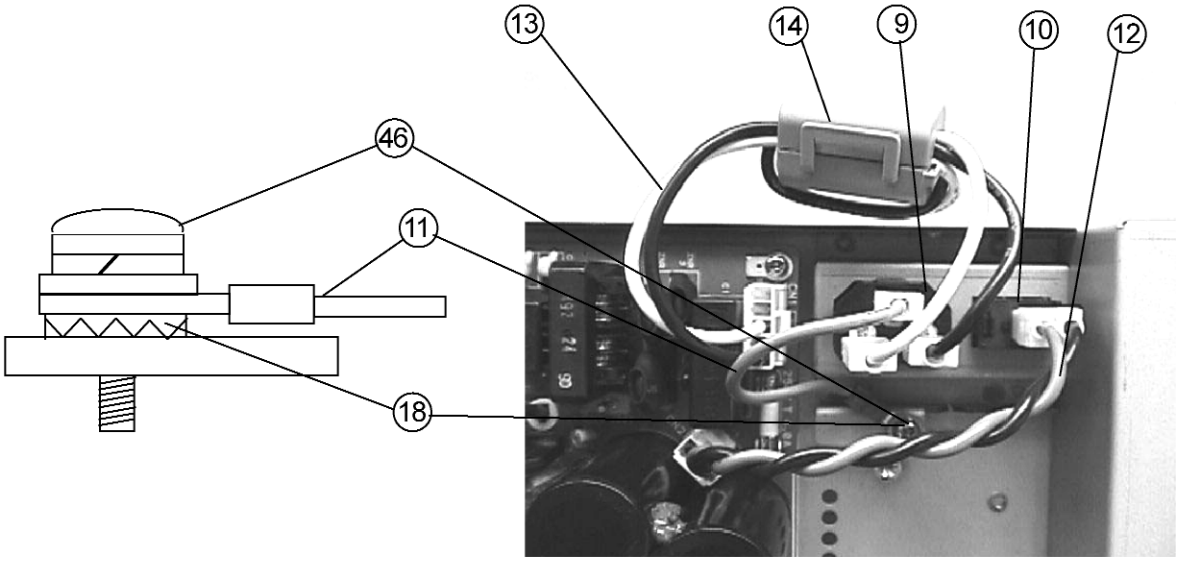

T/P PCB Unit
CN6 on the Main PCB Unit
CN26 on the Main PCB Unit
CN10 on the Main PCB Unit
CN9 on the Main PCB Unit
JDK23900B4
CN14 on the Main PCB Unit
MB PCB Unit
Main PCB Unit
CN22 on the Main PCB Unit
CN19 on the Main PCB Unit
Peripheral PCB Unit

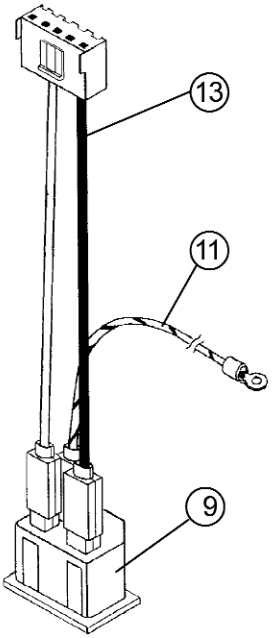
Main PCB (75) Peripherals

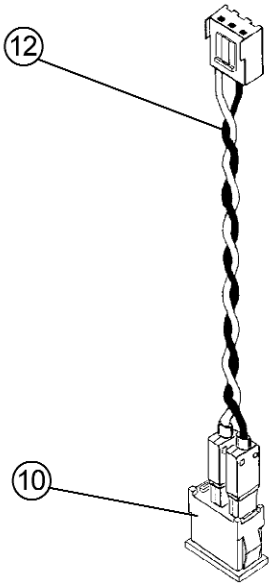


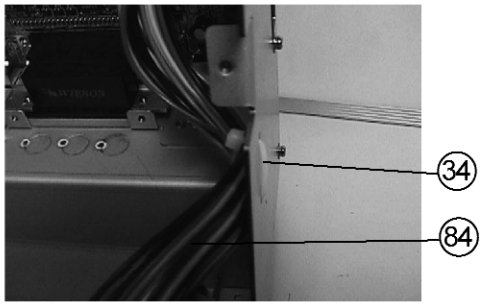


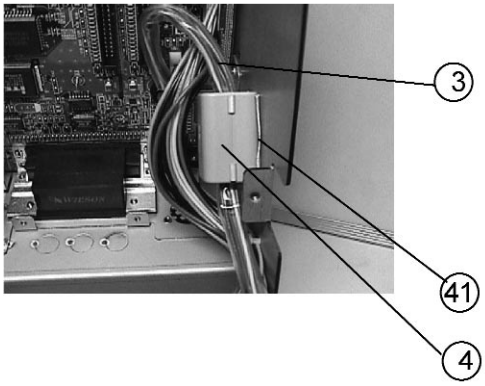
Power Supply Peripherals



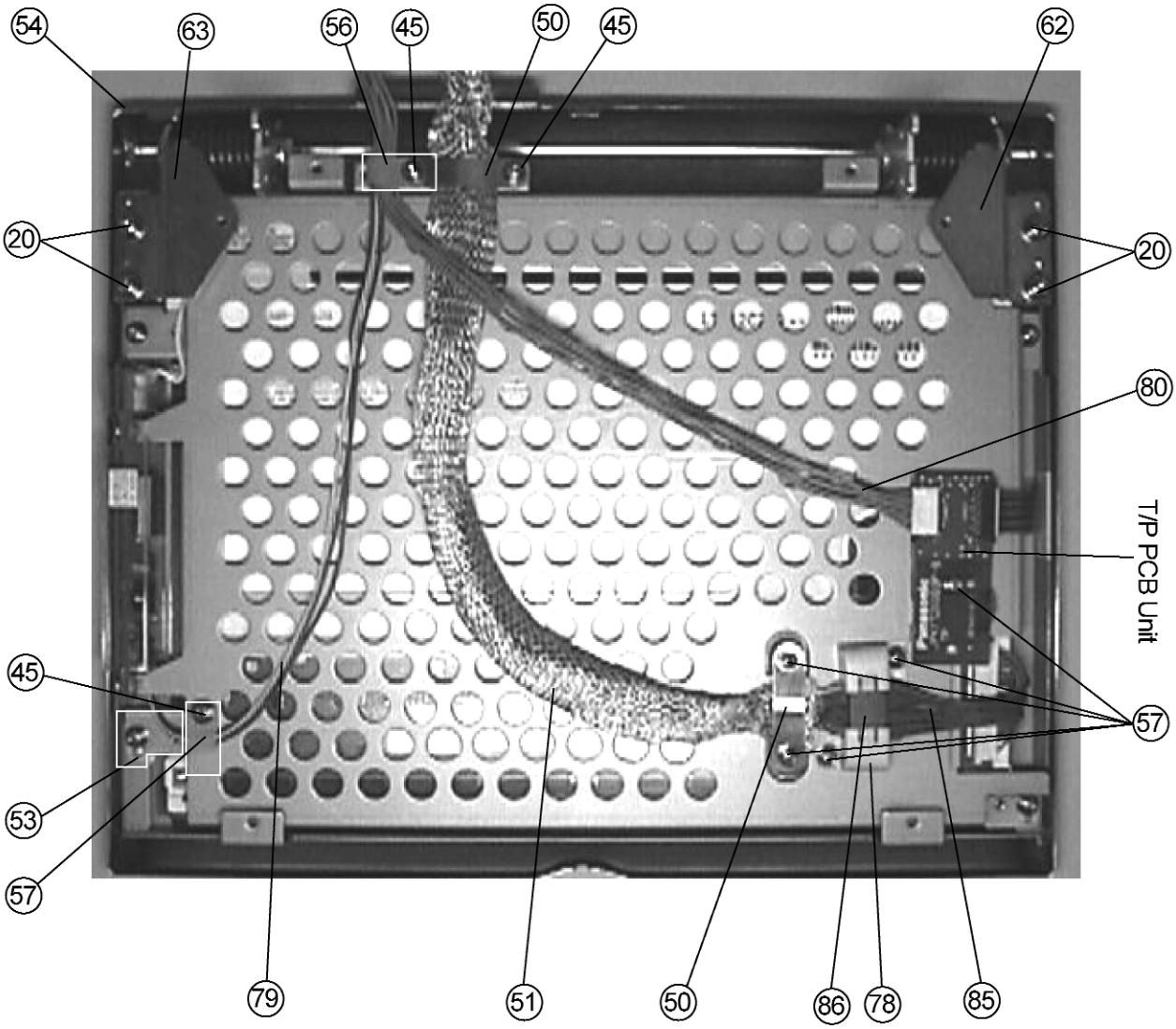




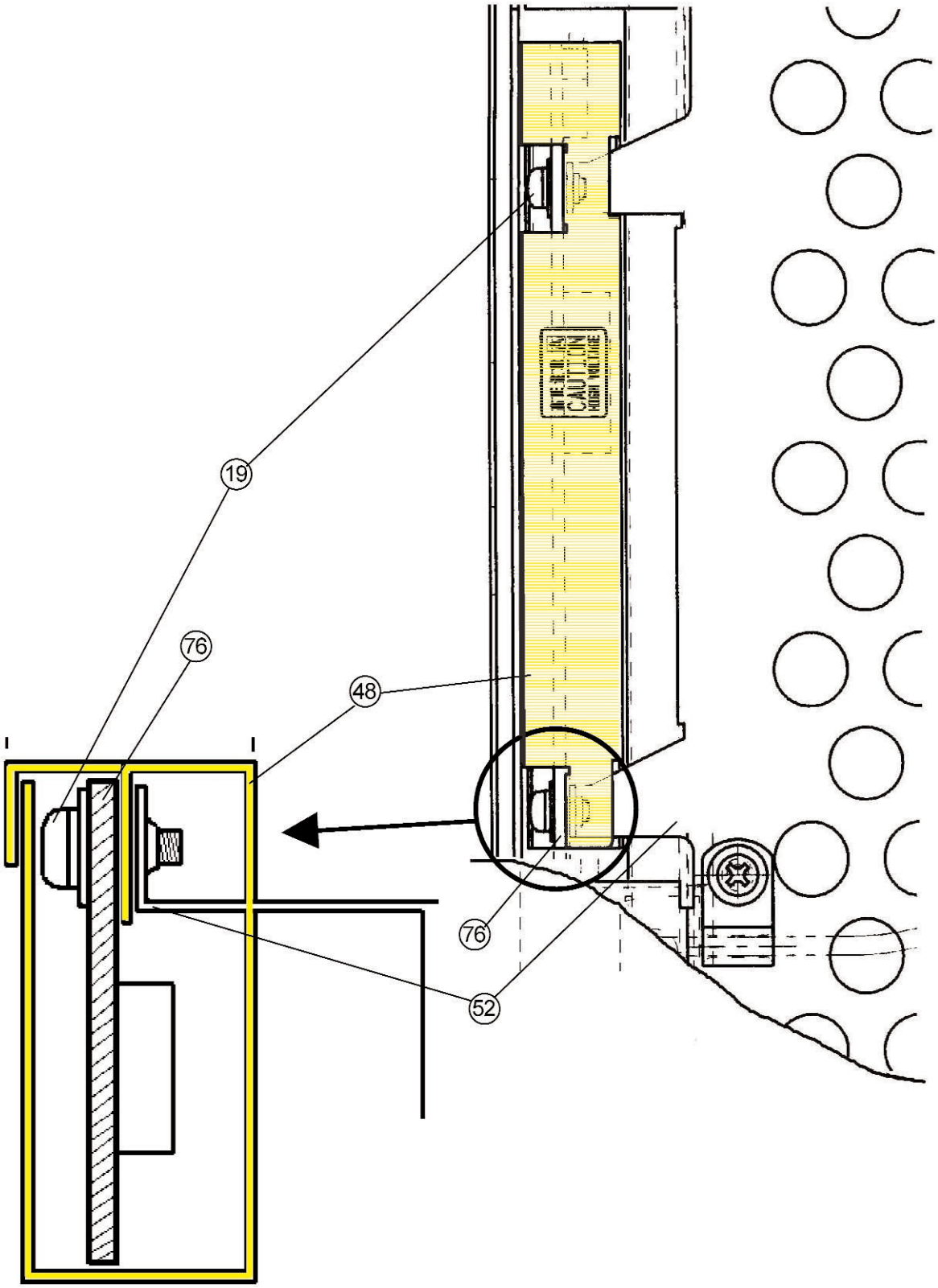



3
41
4

LCD Peripherals



Inverter PCB Peripherals



5.2 Body Block Replacement Parts List

Note: When ordering replacement parts, indecate Part No. and Name of Parts.
RTL mark in Remarks means “Repairable PCB Assembly” “Retention Time Limited”.

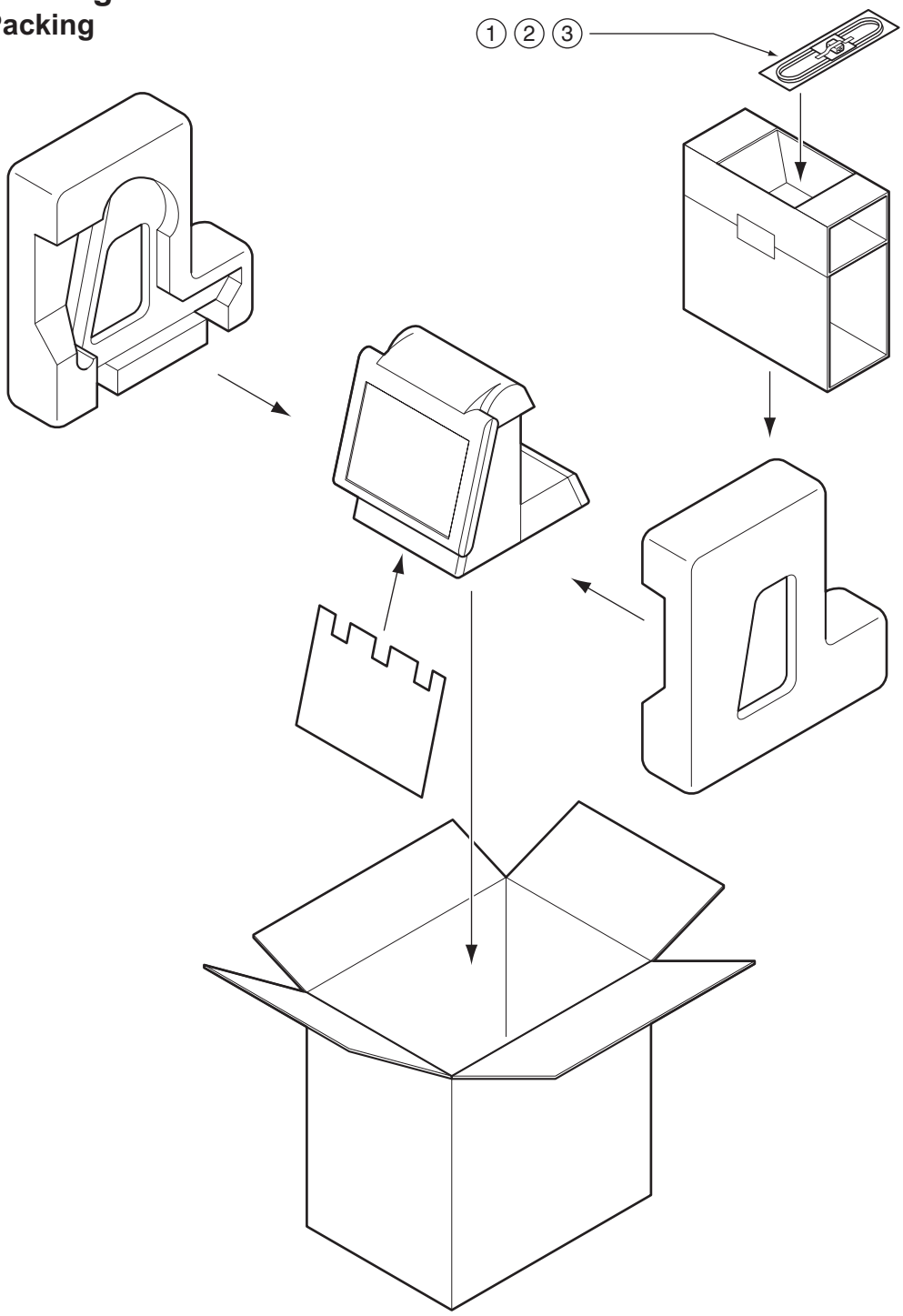
Ref. No.		Part No.	Part Name & Description	Ps/set	Remarks
1		L5BDDDN00001	LIQUID CRYSTAL DISPLAY	1	
2		VNR12C289LU	BACK LIGHT	1	
3		YJJDK23950B4	CABLE	1	
4		YJMSFC8KEX	CHOKE COIL	1	
5		XYN3+F6	TERMINAL SCREW W/WASHER	4	
6		YJJ3A58040B4	DUST PROTECTOR	1	
7		YJJ2T58010B3	MOUNTING BRACKET	1	
8		YJM202MD10BA	CUSTOMER DISPLAY	1	
9		YJ42R0232121	CONNECTOR	1	
10		K0AABE000020	SEE SAW SWITCH	1	
11		YJJDK23400B4	CABLE	1	
12		YJJDK23980B4	CABLE	1	
13		YJJDK23990B4	CABLE	1	
14		YJMSFC8KEX	CHOKE COIL	1	
15		XSB3+20FC	TERMINAL SCREW.STEEL	4	
16		XSB3+6FC	TERMINAL SCREW.STEEL	8	
17		XSB4+6FC	TERMINAL SCREW.STEEL	5	
18		XWC4B	WASHER.STEEL	1	
19		XYN3+F6	TERMINAL SCREW W/WASHER	30	
20		XYN4+F8	TERMINAL SCREW W/WASHER	1	
21		YJJ7C51610B4	PACKING	1	
22		YJJ2P51090B4	INSULATOR.POLYCARBONATE	1	
23		YJJ2N62110B4	SPACER	2	
24		YJJUX30812B3	BASE FRAME ASSY	1	
25		YJJ2T58230B3	MOUNTING BRACKET	1	
26		YJJ2C58250B4	"LOCK PLATE, STAINLESS"	1	
27		YJJ2S58260B4	ANGLE	1	
28		YJJ2S58270B4	ANGLE	1	
29		YJJ2S58280B4	ANGLE	1	
30		YJJ2S58290B4	ANGLE	4	
31		YJSQ-10	SPACER	4	
32		YJNK5N YJNK4N	CORD CLAMPER	1	
33		YJJ5L42550B4	RUBBER FOOT	4	
34		YJPLT-1M	CLAMPER	1	
35		YJSQ-15	STAY	4	
36		YJJ5W42560D3	PANEL	1	
37		KB07K0TEIGUA	ANGLE	2	
38		YJJUX30310B3	HEAT PIPE ASSY	1	
39		YJPLT-1.5M	PANTAI	2	
40		YJRF100	ANGLE	2	
41		YJJ1D04150B4	ADHESIVE	1	
42		XSB3+6FC	TERMINAL SCREW.STEEL	12	
43		XSB3+8FC	TERMINAL SCREW.STEEL	1	
44		XYN3+F6	TERMINAL SCREW W/WASHER	12	
45		XYN3+F8	TERMINAL SCREW W/WASHER	2	
46		XYN4+F8	TERMINAL SCREW W/WASHER	8	

Ref. No.		Part No.	Part Name & Description	Ps/set	Remarks
47		YJJ3A59590B4	DUST PROTECTOR	2	
48		YJJ2P58140B4	INSULATOR	1	
49		YJJ2W58101B2	FRAME	1	
50		YJJ2C51250B4	LOCK PLATE.STAINLEES	3	
51		YJJ2H57660B4	MAGNETIC SHIELD	1	
52		YJJ2H59410B2	"MAGNETIC SHIELD,STAINLESS"	1	
53		YJJ2P62100B4	INV SHEET	1	
54		YJJ5K42440B2	DISPLAY CASE	1	
55		YJJ5K42450B2	DISPLAY CASE	1	
56		YJNK-3N	CORD CLAMPER	2	
57		YJNK2N	CORD CLAMPER	1	
58		YJJ3G58310B4	RUBBER	2	
59		YJJ7S49510B4	CAUTION LABEL	1	
60		YJJ2F59480B4	CUSHION	1	
61		YJJ6E55900B3	SHEET	1	
62		YJJUX29830B3	HING-STAY	1	
63		YJJUX29840B3	HING-STAY	1	
64		YJP7FRE20WA1	TOUCH PANEL UNIT	1	
65		XSB3+6FC	TERMINAL SCREW.STEEL	15	
66		XYN3+F6FX	TERMINAL SCREW W/WASHER.STEEL	3	
67		YJJ2H58150B3	MAGNETIC SHIELD	1	
68		YJJ2H59570B4	MAGNETIC SHIELD	1	
69		YJJ2H59621B4	MAGNETIC SHIELD	5	
70		YJJUE29881B3	REAR COVER ASSY	1	
71		YJJ5E42480E1 YJJ5E42480F1	TOP COVER	1	Gxx
72		YJJ5E42520D2 YJJ5E42521E2	CTM-DSP COVER	1	Gxx
73		YJJ5E42530D3	COVER	1	
74		YJJ5K42490D1	FRONT COVER	1	
75		YJP7FRF241H	MAIN PCB	1	RTL
76		MTIV-121TFT	INVERTER	1	
77		M0CC00000016	HDD	1	
78		YJFRH-12	HOLDER	2	
79		YJJDK23860B4	CABLE	1	
80		YJJDK23880B4	CABLE	1	
81		YJJDK23910B4	CABLE	1	
82		YJJDK23920B4	CABLE	1	
83		YJJDK23930B4	CABLE	1	
84		YJJDK23940B4	CABLE	1	
85		YJJDK24020B4	CABLE	1	
86		J0KD00000014	NOISE FILTER	1	
87		JUS40201B4	POWER SUPPLY UNIT	1	
88		N4HKLNB00004	BATTERY	1	
89		YJJ2R58050B4	BATTERY CASE	1	
90		XYN4+F8	TERMINAL SCREW W/WASHER	2	
91		YJJ2X58071B4	BATTERY COVER	1	
92		YJJ2F58060B4	CUSHION	1	
93		XWG3NY-CA-B	NYLON WASHER	2	
94		XTB3+10G	SCREW	7	
95		YJJ6G55010B4	BATTERY PLT	1	

Ref. No.		Part No.	Part Name & Description	Ps/set	Remarks
96		YJJDK265000B4	BATTERY CABLE	1	
97		YJJ5L40310B4	RUBBER FOOT	2	
98		YJJ2S70040B4	CONNECTOR BRACKET	1	
99		YJP7FRJ20P3H	MB PCB	1	RTL
100		YJP7FRJ20P1H	PERIPHERAL PCB	1	RTL

6 Packing

6.1 Packing



Ref. No.		Part No.	Part Name & Description	Ps/set	Remarks
1		YJMSFC5EX	CHOCK COIL	1	Axx/Exx/Gxx/Sxx/Wxx
2		K2CG3EW00001	AC CORD	1	Axx
		YJKP30EPHA			Exx
		YJJDA30770B4			Fxx/Gxx
		YJJDK13920B4			Uxx/Cxx
		YJKPSV2516Y			Wxx
3		YJPLT-1M	CLAMPER	1	Axx/Exx/GxxSxx

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